Recent developments in paradise: fast waveform sampling readout electronics for finely pixelated photosensors in Hawaii

Nalu Scientific

Data Acquisition Systems

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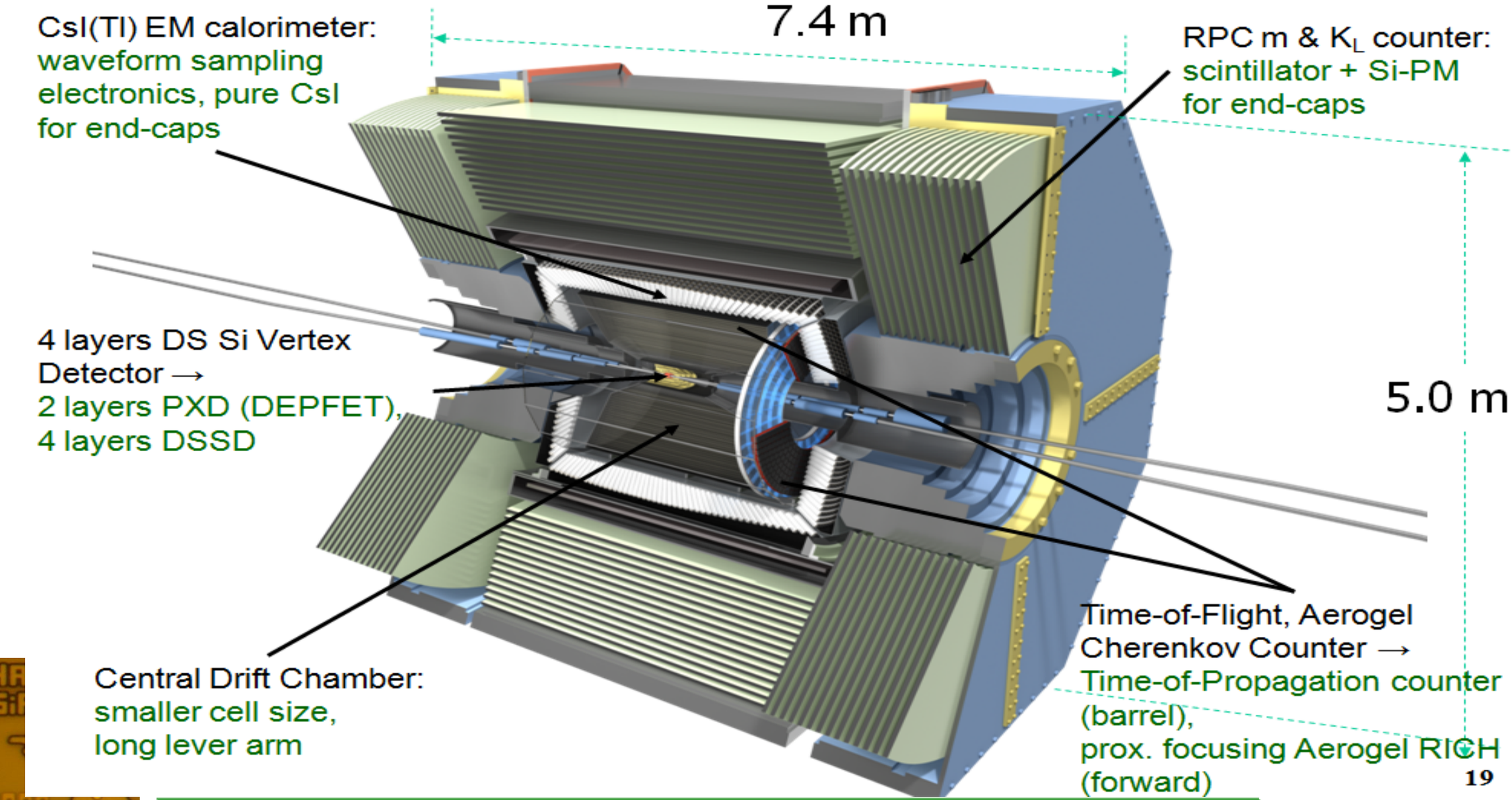
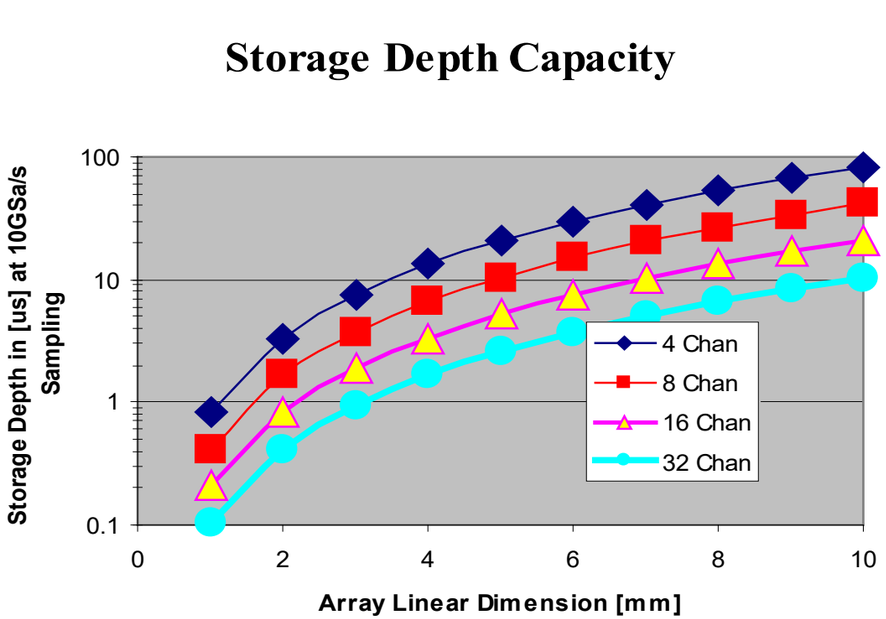
Belle II detector – TOP & Scint readout

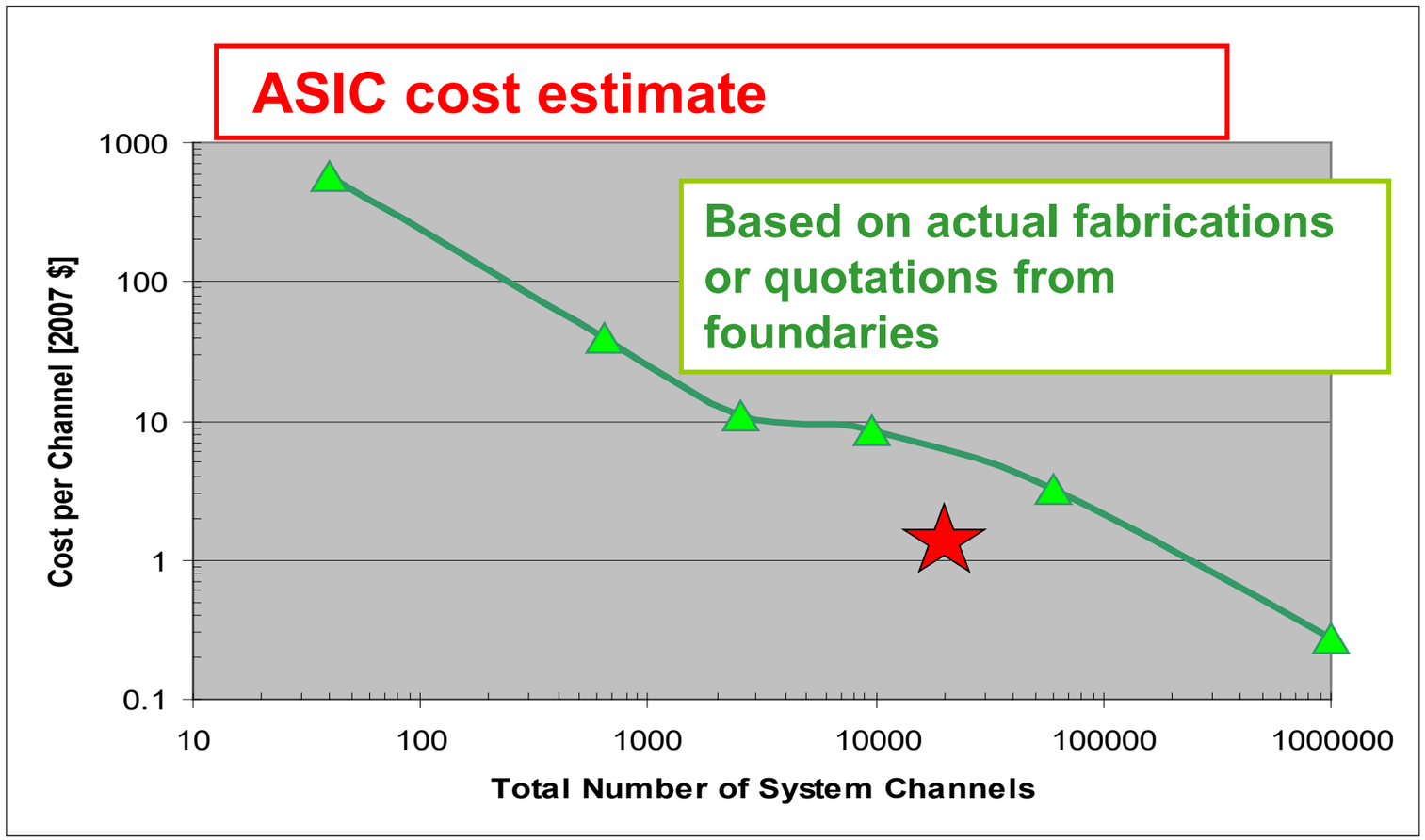


Looking back on >10 year development

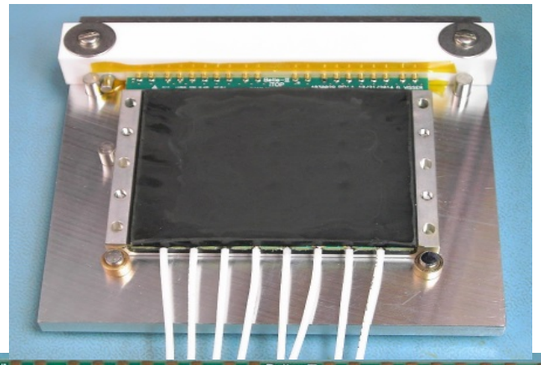
- ASIC costing well understood, very competitive!

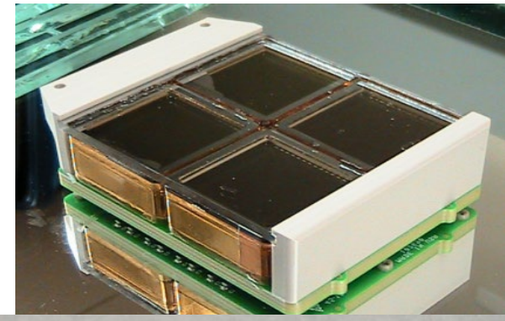
NIM A591 (2008) 534-345.

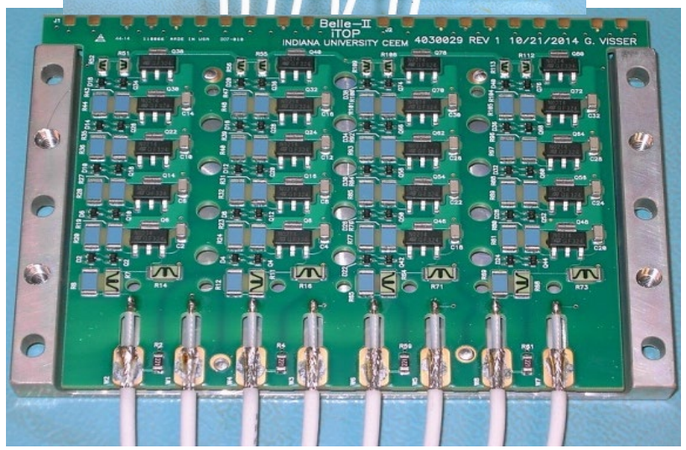


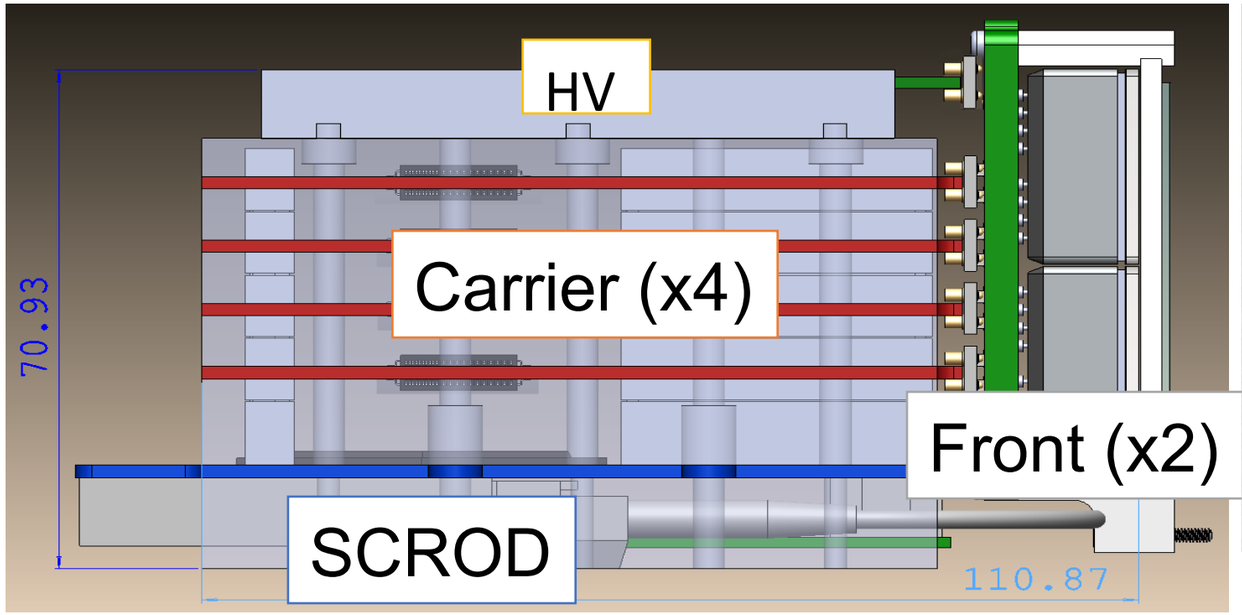


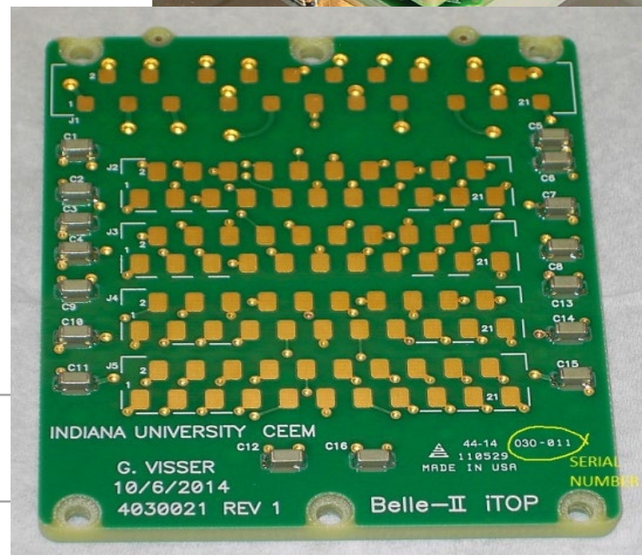
iTOP Readout “boardstack”
(1 of 4 per TOP Module)

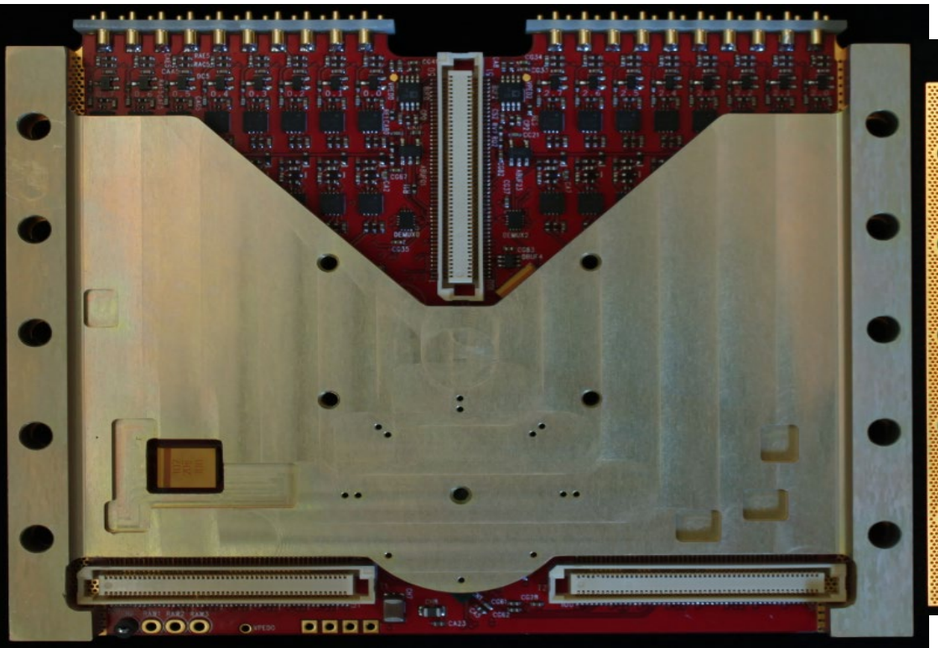


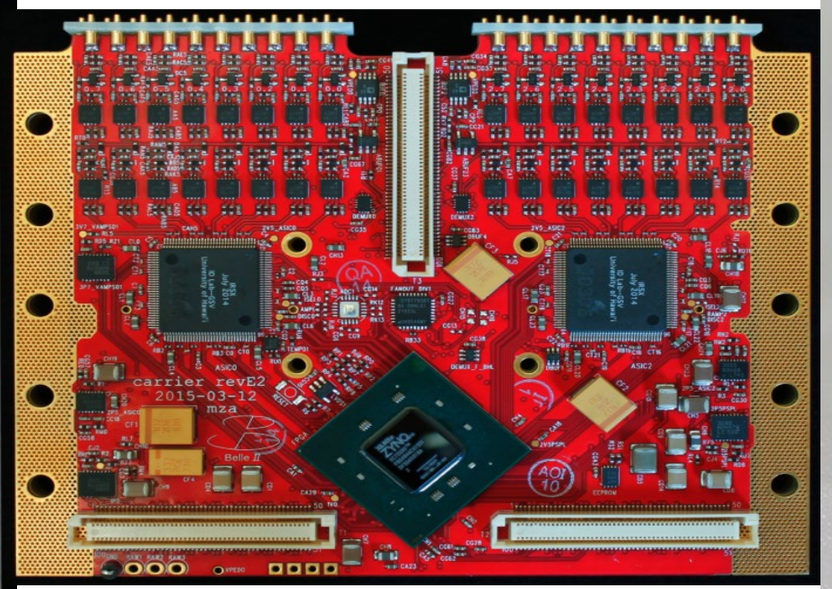


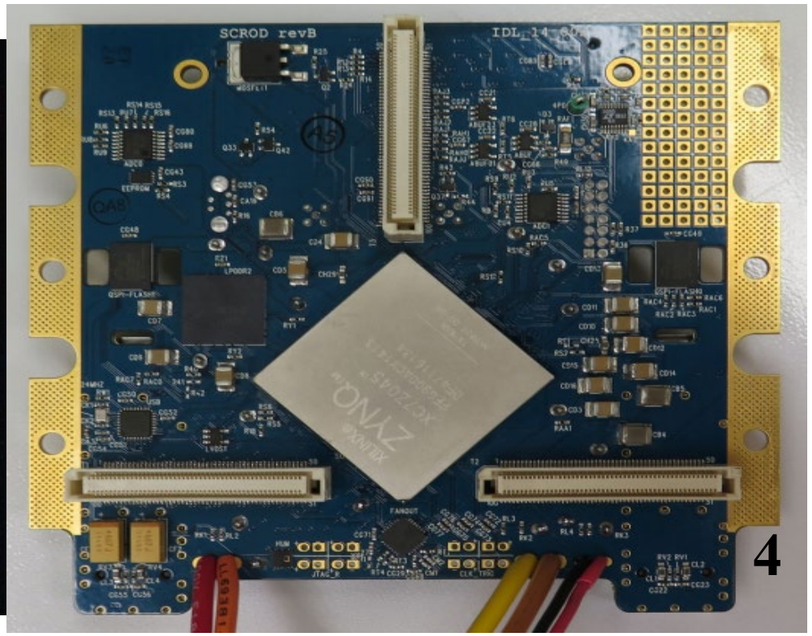




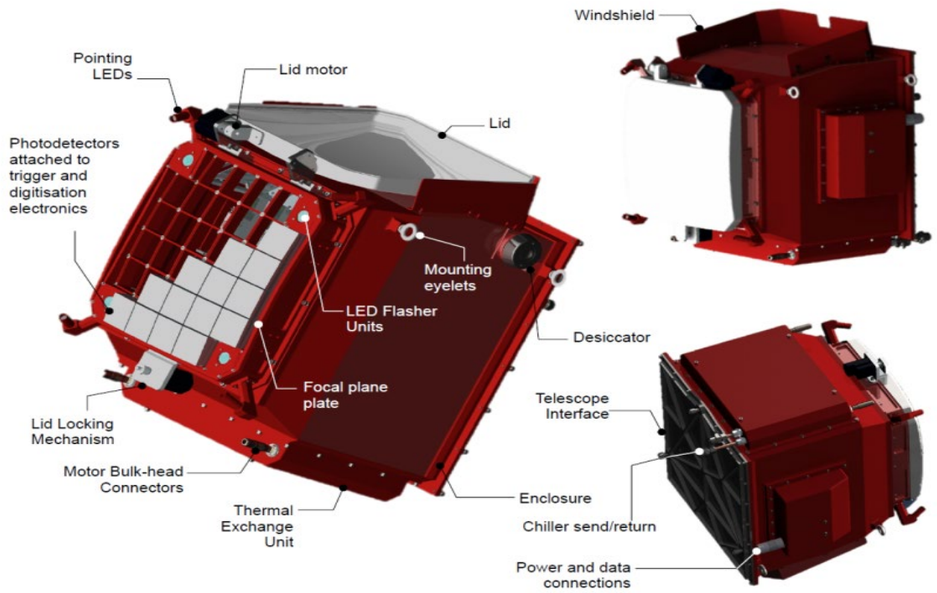


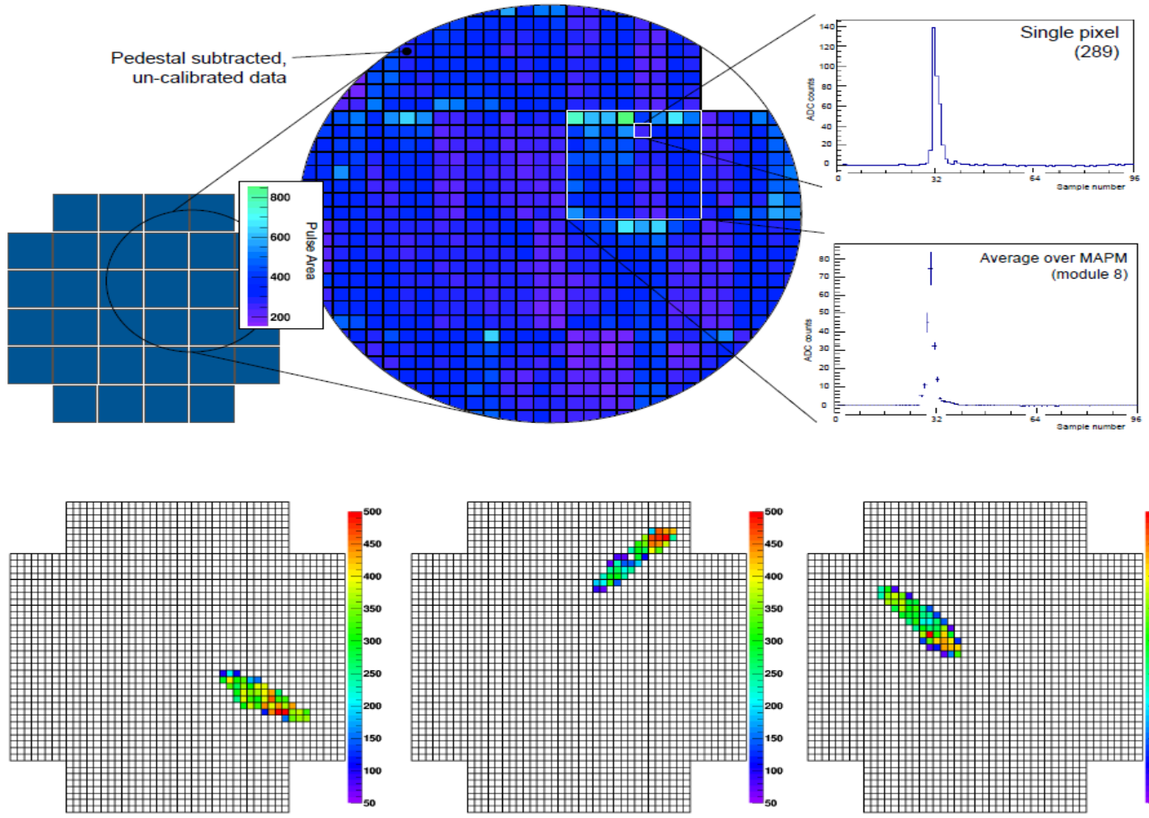


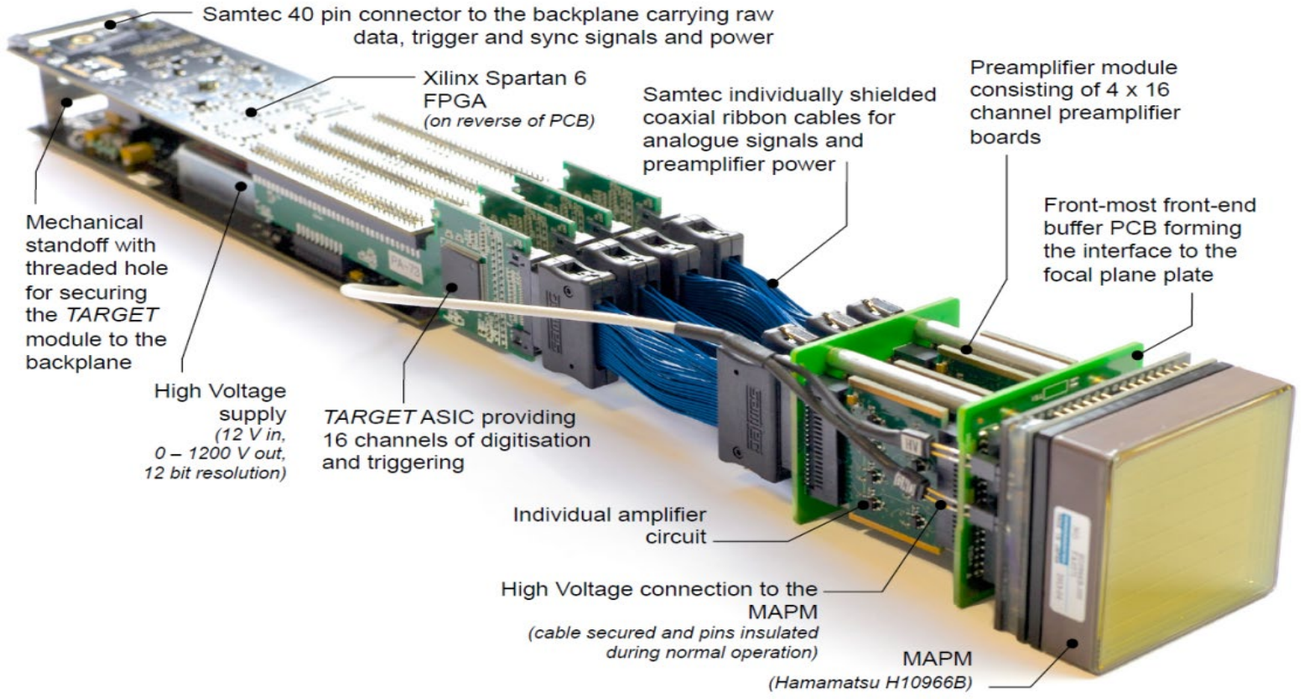


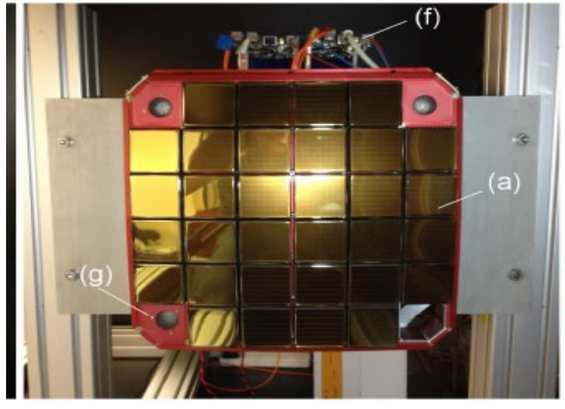


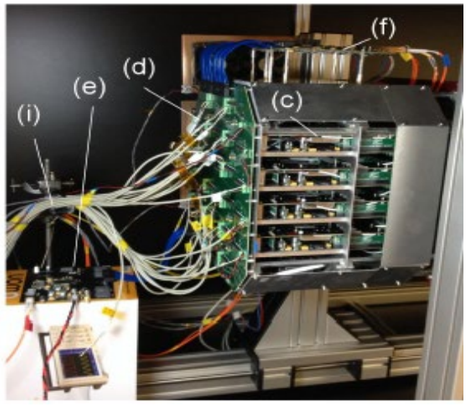
GCT Camera (CTA) – another TARGET application



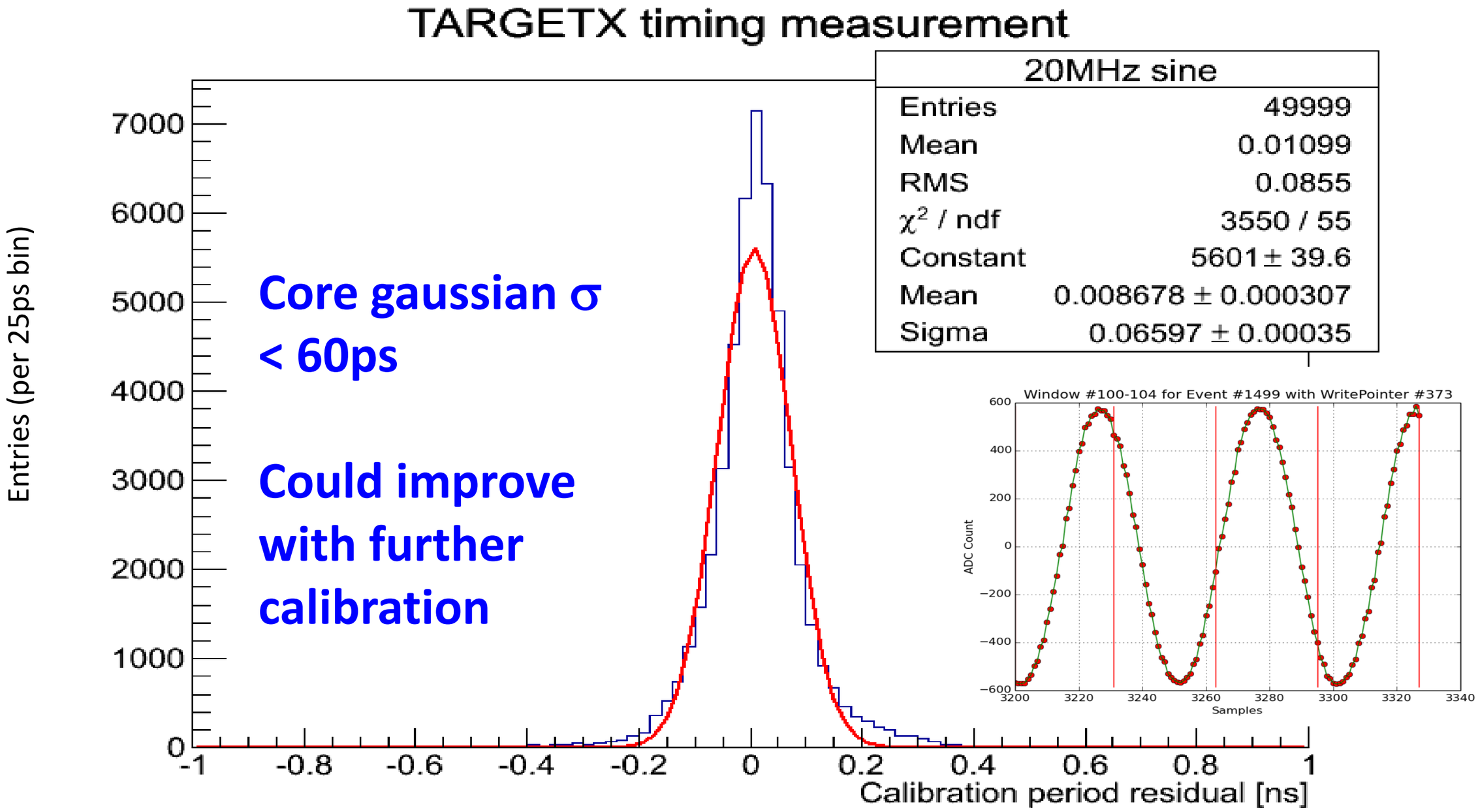






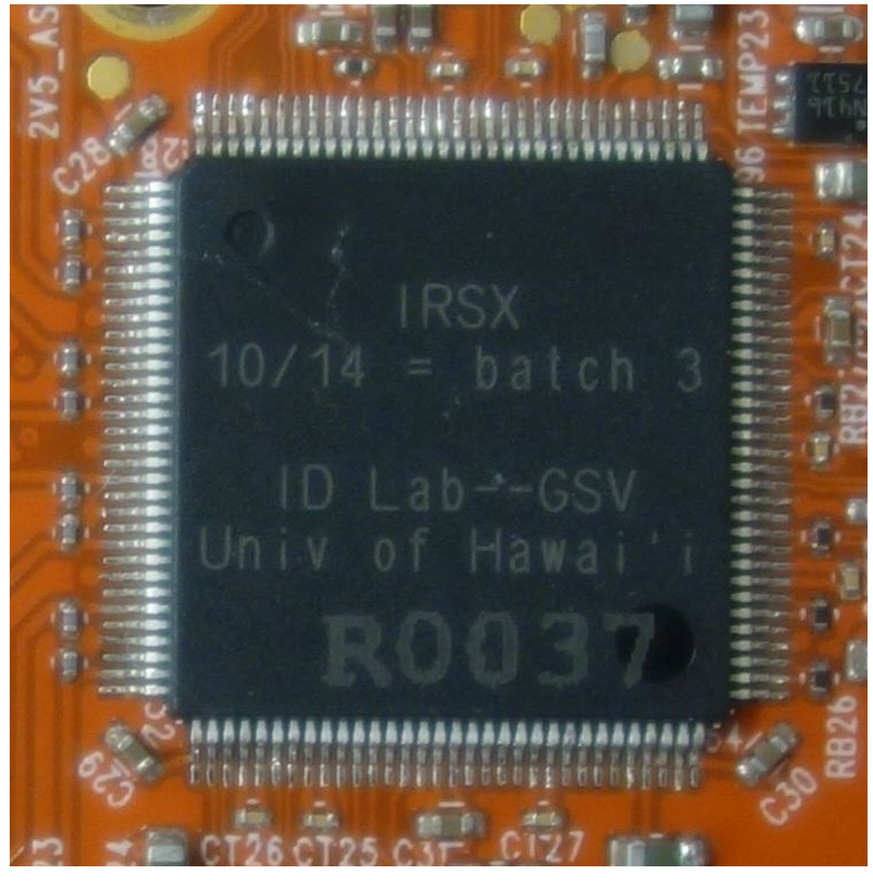


Timing example (only 1 GSPS)



Readout: Precision Timing Electronics

- Consider the IRSX ASIC
  - Designed by IDLAB, UH
- Operated at 2.7GSa/s in TOP
  - ~600MHz analog bandwidth
  - 32k analog buffer cells (~10us)
  - 12 bit digitisation w/o deadtime
- Power budget ~600mW/ch
  - ASIC: ~125mW/ch
  - Preamp: ~150mW/ch
  - FPGAs: ~300mW/ch



Messages going forward

- Performance OK, but reducing power important
- Ideally integrate any needed amplification
- ASIC development important, but firmware and support have been the most critical issues
- Very inefficient to have control from external FPGA
- Integrated needed DACs, triggering, pedestal correction and feature extraction will be key to reducing overall system costs and pushing higher integration density

Challenges and Opportunities

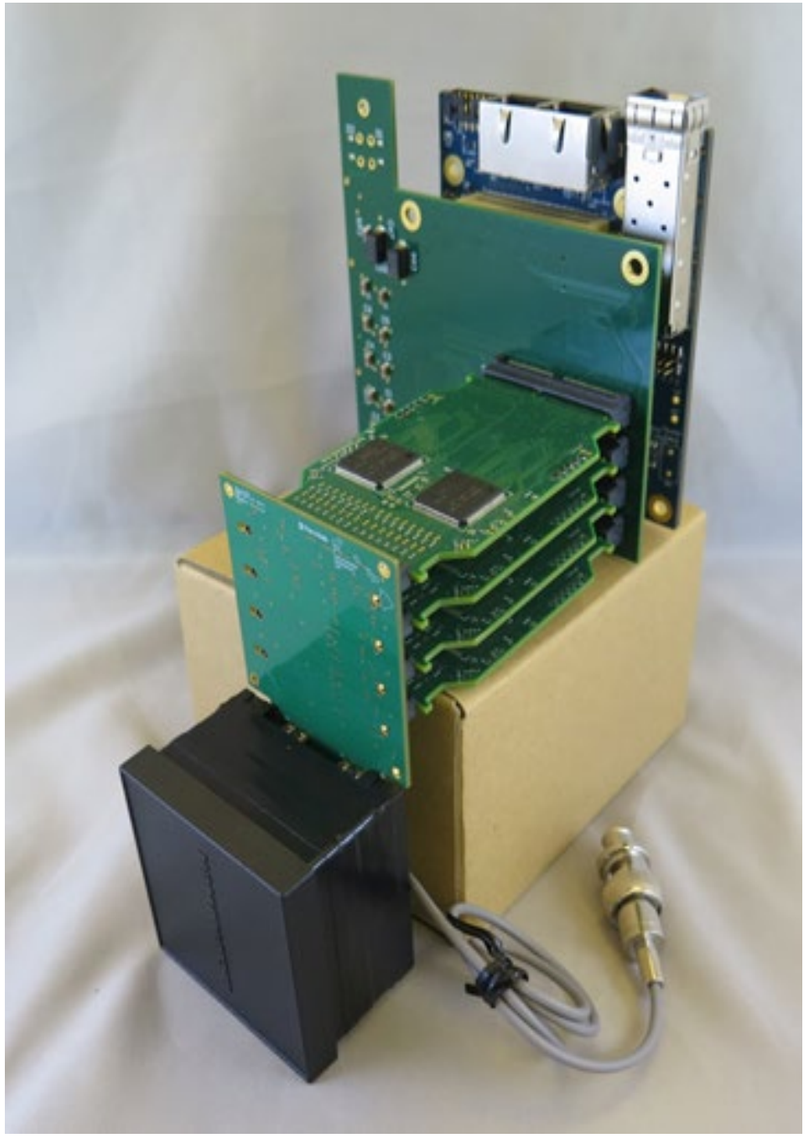
Challenges

- Need to read out several photosensors (MaPMTs, MCP-PMTs, and SiPMs) with similar sensor and pixel size (16x16 array of 3 mm pixels)
  - DIRC also requires good timing (<100 ps)
- Goal is to have common front end electronics with good timing that can be used with many sensors and detectors
- Even finer pixel pitches being considered

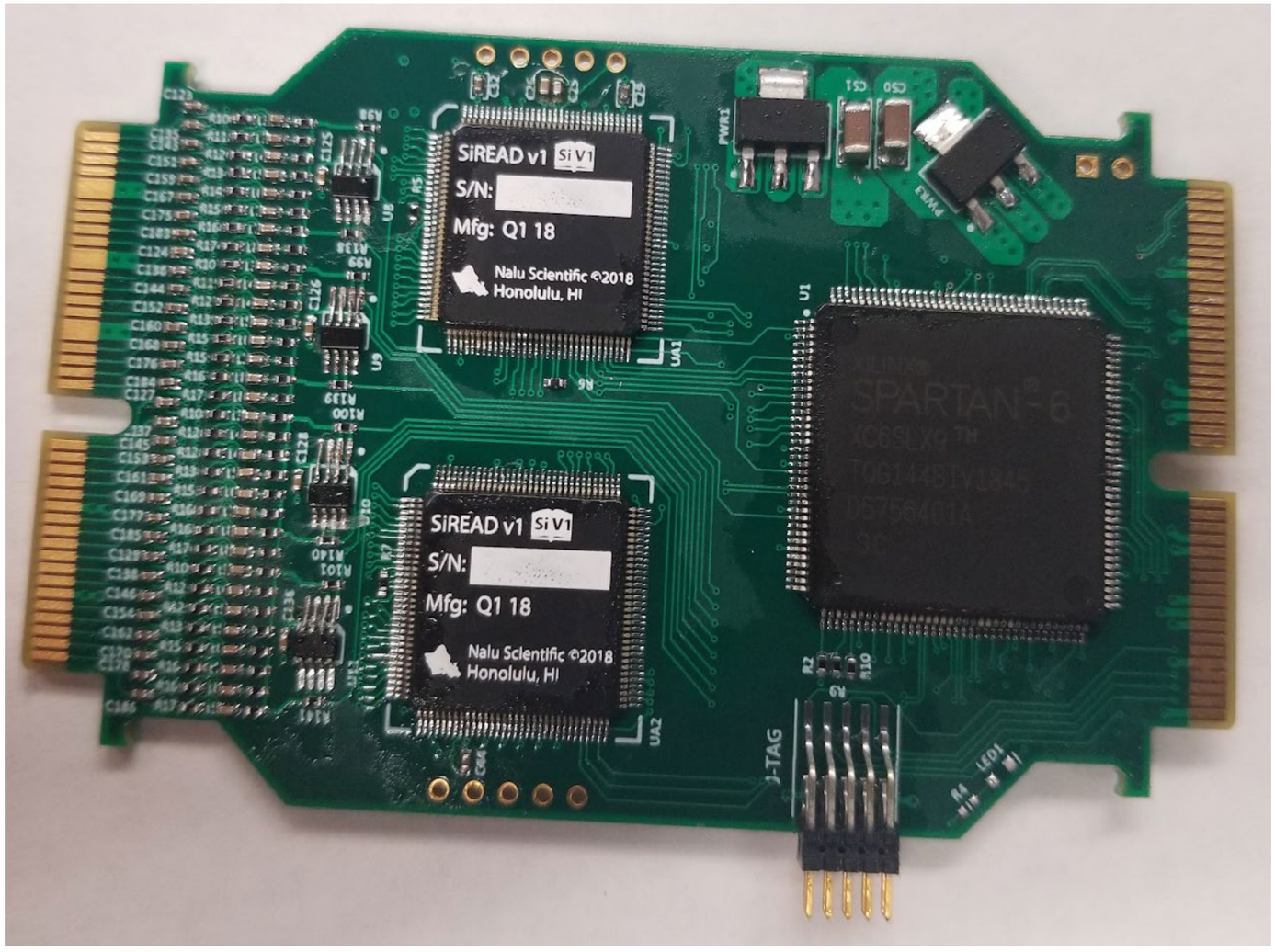
Opportunities

- Smaller technology nodes offer
  - Higher gain-bandwidth amplifiers, reduced capacitance
  - Integration of significant amounts of digital memory and processing capabilities
- High-speed serial I/O, for compact control/data collection
- Collaboration between Univ. Of Hawaii and Nalu Scientific
  - Able to supply these ASICs commercially
  - Engineering support for designs

MA PMT Readout eRD-14



Photograph of the first generation of 256-anode 2" PMT readout for use with mRICH prototype in the Fermilab beam test facility.



Photograph of the 64 channel SiREAD based (2x SiREAD rev.1) readout card as a building block for the 256 MA-PMT readout.

Benefits of Higher Integration - SoC

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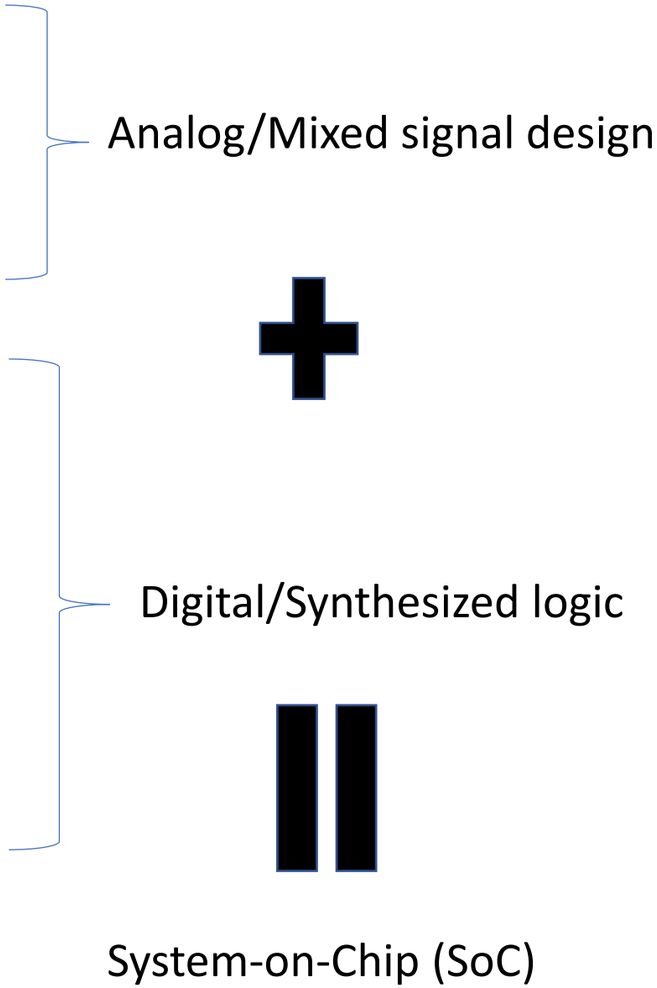
- **Analog memory:**
  - Sampling always on (1-10 Gsa/s), but at low power
  - Digitize only Region of Interest (ROI)
  - Long analog buffer -> suitable for large experiments
- **Digital processing:**
  - Per channel cost reduction by a factor of 4
  - Relax thermal design by 40% reduction in power dissipation
  - Trigger time-stamping at the front-end
  - Eliminating the need for costly high-end FPGAs
  - User friendly: substantially reducing the FPGA firmware development labor
  - Reduced complexity and design and cabling effort/cost for the front-end boards



Nalu Scientific SBIR Project: ASoC

Compact, high performance waveform digitizer

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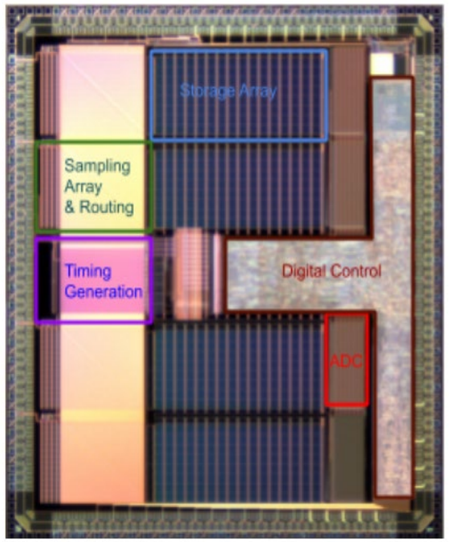
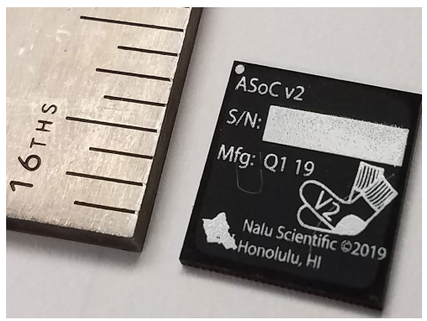
Data Acquisition Systems



Fabricated

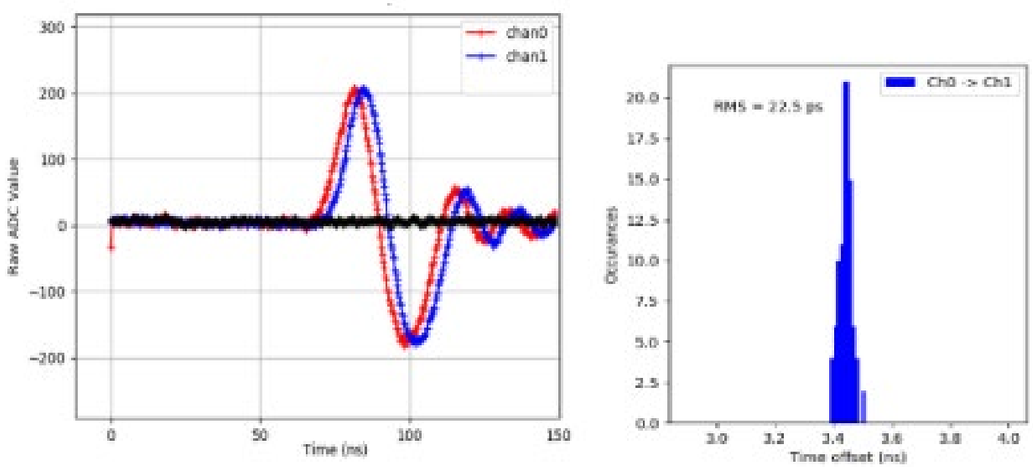


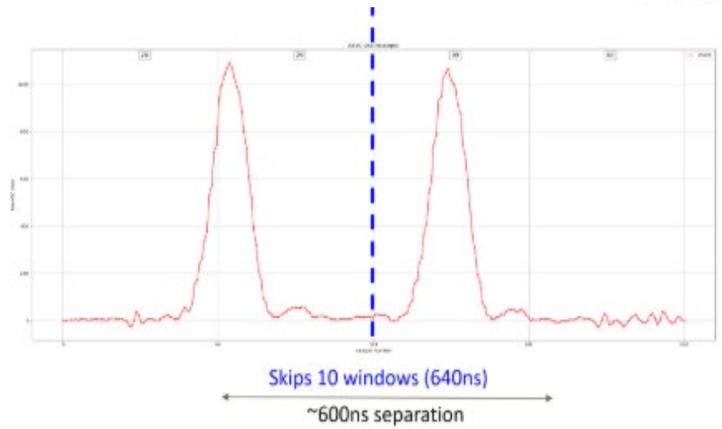
Parameter	Spec (measured)
Sample rate	2.4-3.2GSa/s
Number of Channels	4
Sampling Depth	16kSa/channel
Signal Range	0-2.5V
Resolution	12 bits*
Supply Voltage	2.5V
RMS noise	~1 mV
Digital Clock frequency	25MHz
Timing resolution	<25ps**
Power	140mW/channel
Analog Bandwidth	950MHz

Key Contribution:

- High performance digitizer: 3+ GSa/s
- Highly integrated
- Commercially available
- 5mm x 5mm die size

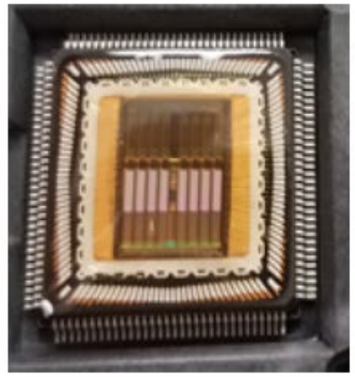
Live demo at IEEE NSS-MIC 2018

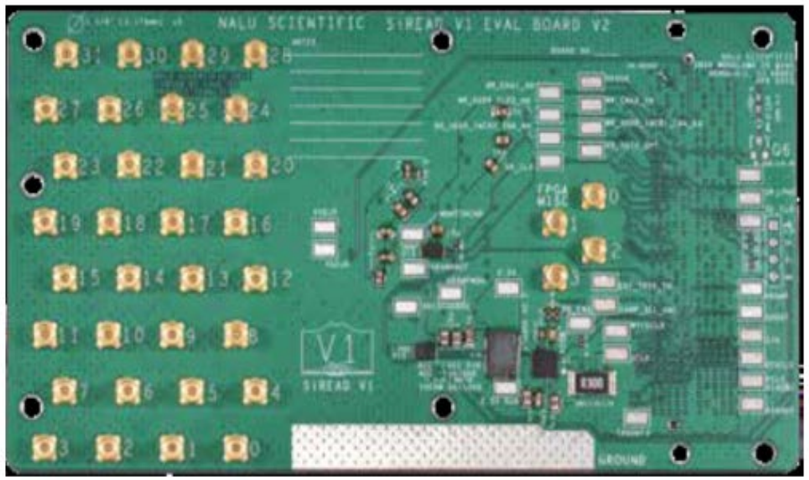


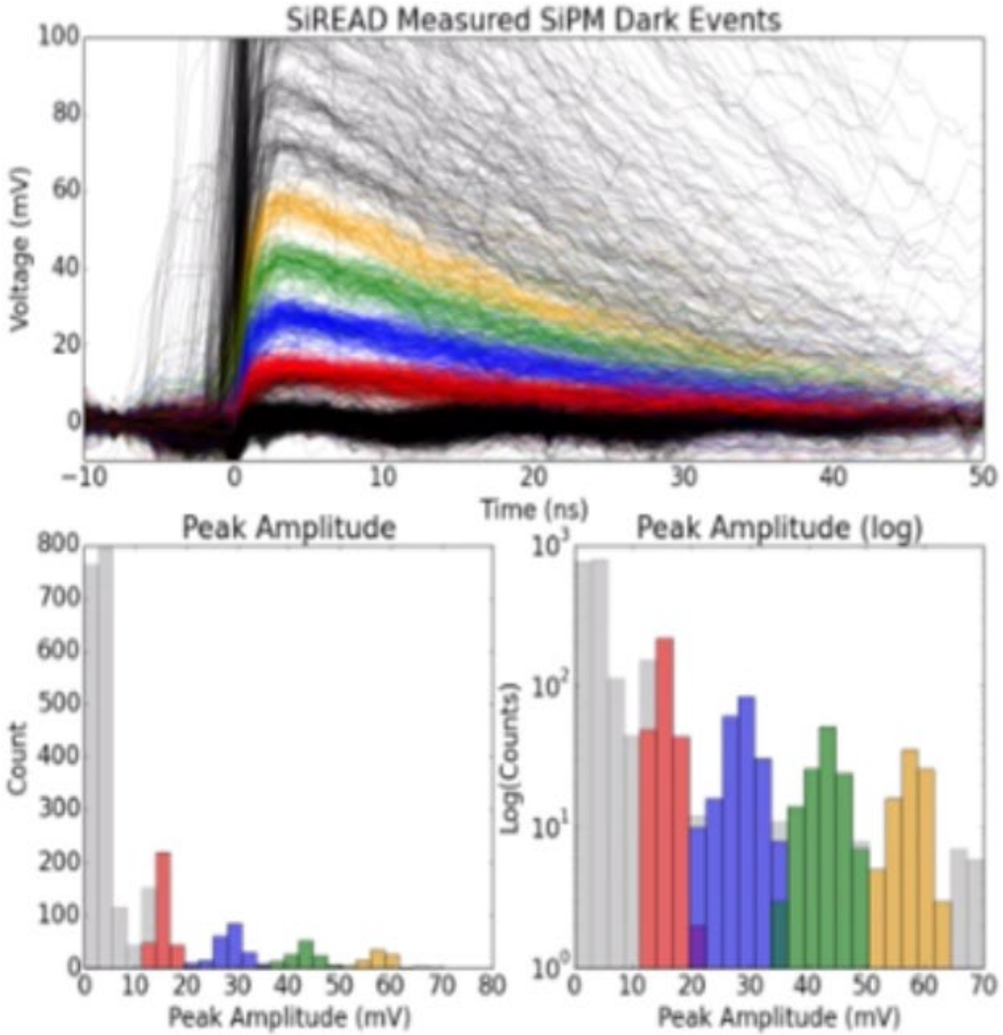


All chips, are designed with commercial grade tools and licenses and can be sold once commercialized.

SiREAD Performance







- Micrograph of the fabricated prototype SiREAD (**top left**). Prototype SiREAD on the evaluation PCB (**top middle**). Superimposed dark count waveforms recorded from a SiPM using the SiREAD operating at 1 Gsa/s (**right**). High channel count evaluation PCB for SiREAD with 32 dedicated MMCX connectors (**bottom left)**.

AARDVARC V2 under test

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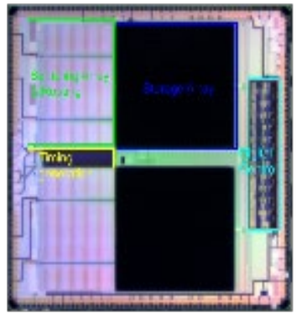
- Test board V2 designed, fabricated and assembled
- Lower cost FPGA dev card identified and made available
- Test firmware V2 developed
- New software and GUI designed and implemented

AARDVARC Parameter	Specification (measured)
Process node	130 nm
Channels	4
Sampling Rate	10-14.5GSa/s*
Storage Samples/ch	32768
Analog BW	>1GHz**
Dynamic Range	1.0 V**
Time accuracy	<5 ps***
Readout	Parallel/Fast Serial
ADC bits	12
Power/ch	80 mW*

AARDVARC Test card

Xilinx A7 FPGA dev card

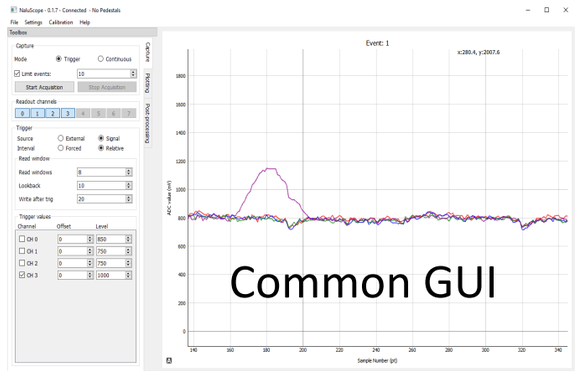


Results to be presented at IEEE NSS- MIC in Manchester

SBIR Data Rights.

14

Current SoC-ASIC Projects



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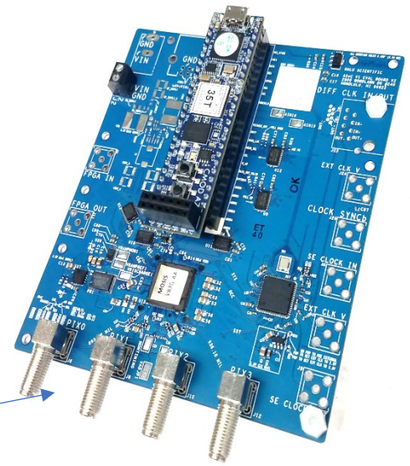
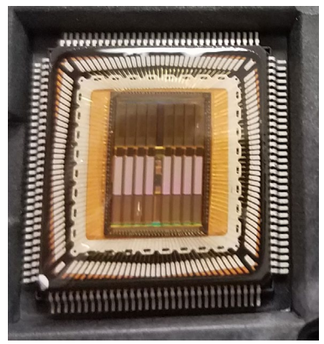
Project	Sampling Frequency (GHz)	Input BW (GHz)	Buffer Length (Samples)	Number of Channels	Timing Resolution (ps)	Available Date
ASoC	3-5	0.8	32k	8	35	Rev 2 avail
SiREAD	1-3	0.6	4k	64	80-120	Rev 1 avail
AARDVARC	6-10	2.5	32k	4-8	4-8	Rev 2 avail
AODS	1-2	1	8k	1-4	100-200	Nov 2019



- **ASoC**: Analog to digital converter System-on-Chip
- **SiREAD**: SiPM specialized readout chip with bias and control
- **AARDVARC**: Variable rate readout chip for fast timing and low deadtime
- **AODS:** Low density digitizer with High Dynamic Range (HDR) option



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Development Complementarity, going forward

- **Exploring higher channel density ASICs for applications such as 64x64 anode readout at Univ. of Hawaii**
- **Once have a viable concept demonstrator, clear path to commercialization via Nalu Scientific**
- **UH provides comprehensive bench, environmental and picosecond laser/photosensor testing**
- **Nalu provides commercial grade ASICs with professional engineering and support**
- **Expect to continue to push boundaries of throughput, timing, channel density and ease-of-use**