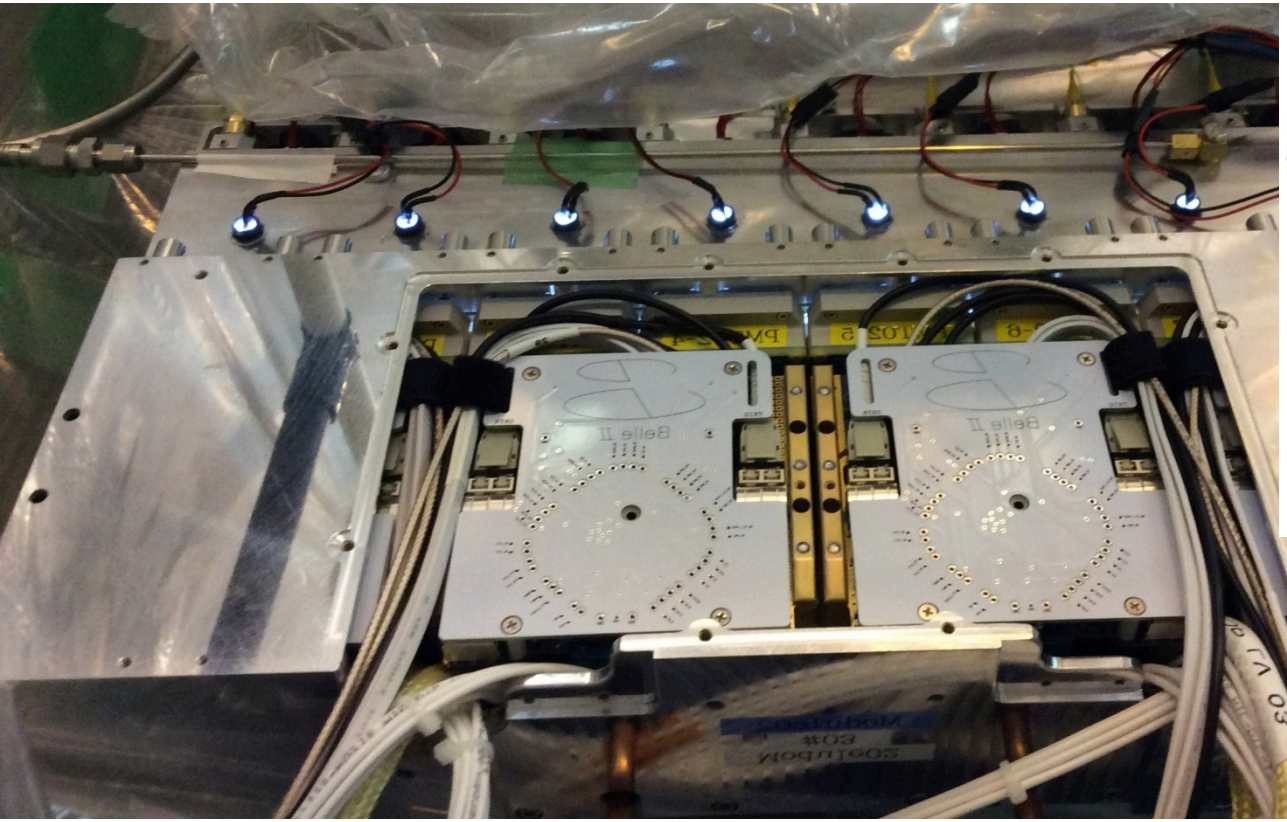
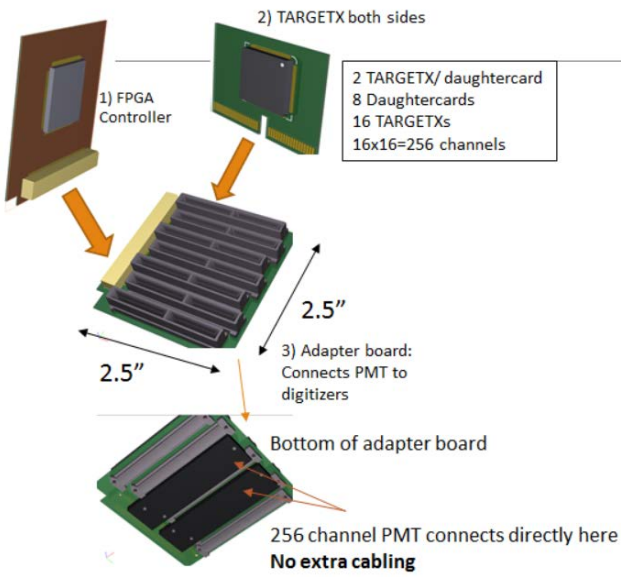
Waveform Sampling Readout – Lessons from the Belle II TOP and applications to future DIRC detectors





Gary S. Varner

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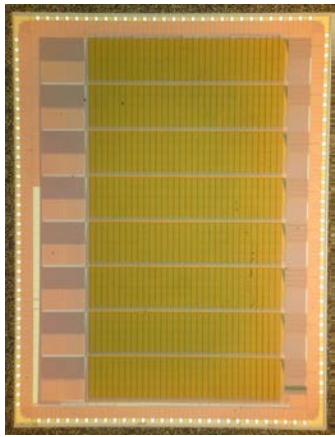
DIRC2017, Castle Rauischholzhausen

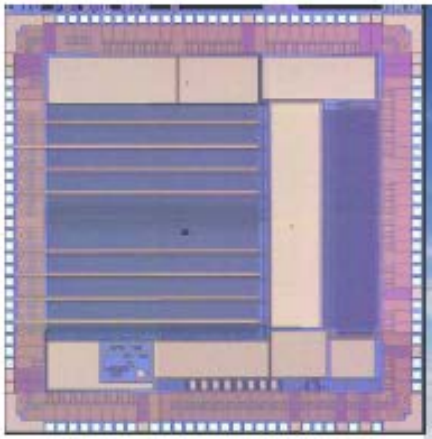


Overview

- State-of-the-art DIRC (RICH) detectors
  - Readout (needs to be) increasingly integrated
  - Finer resolution (spatial, timing) ➔ higher channel density
- Highly integrated readout
  - Reduces system cost (cables can dominate)
  - Improved modularity/performance
- A couple examples:
  1. Recently deployed DIRC system (Belle II TOP)
  2. High precision timing **(latest)**
  3. Low-cost, high density, next generation readout

Waveform Sampling: An Enabling Technology

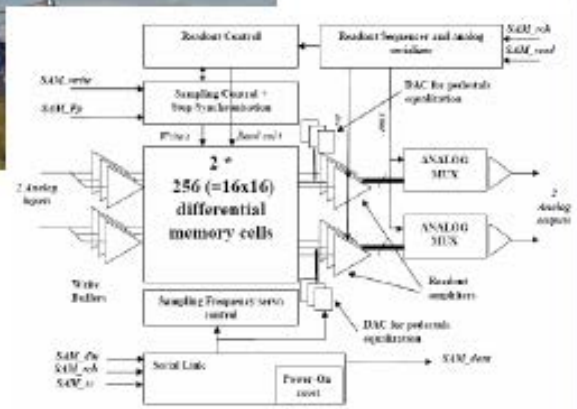
- **ATWD – IceCube**

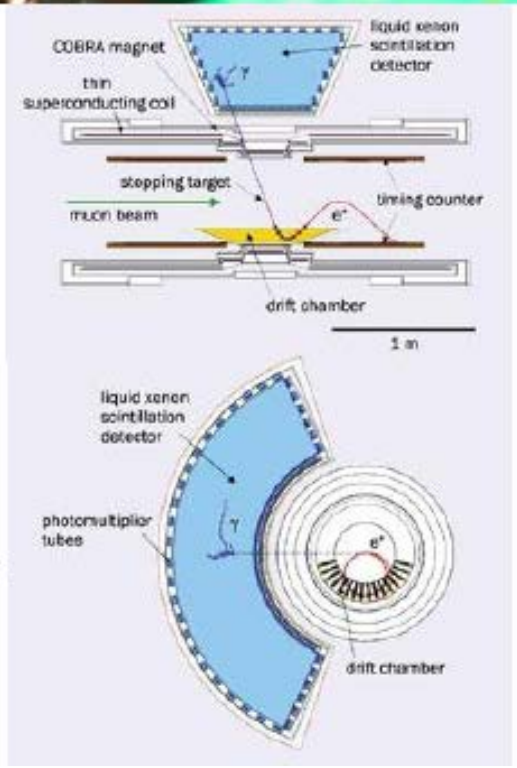


LABRADOR3,
ANITA Experiment

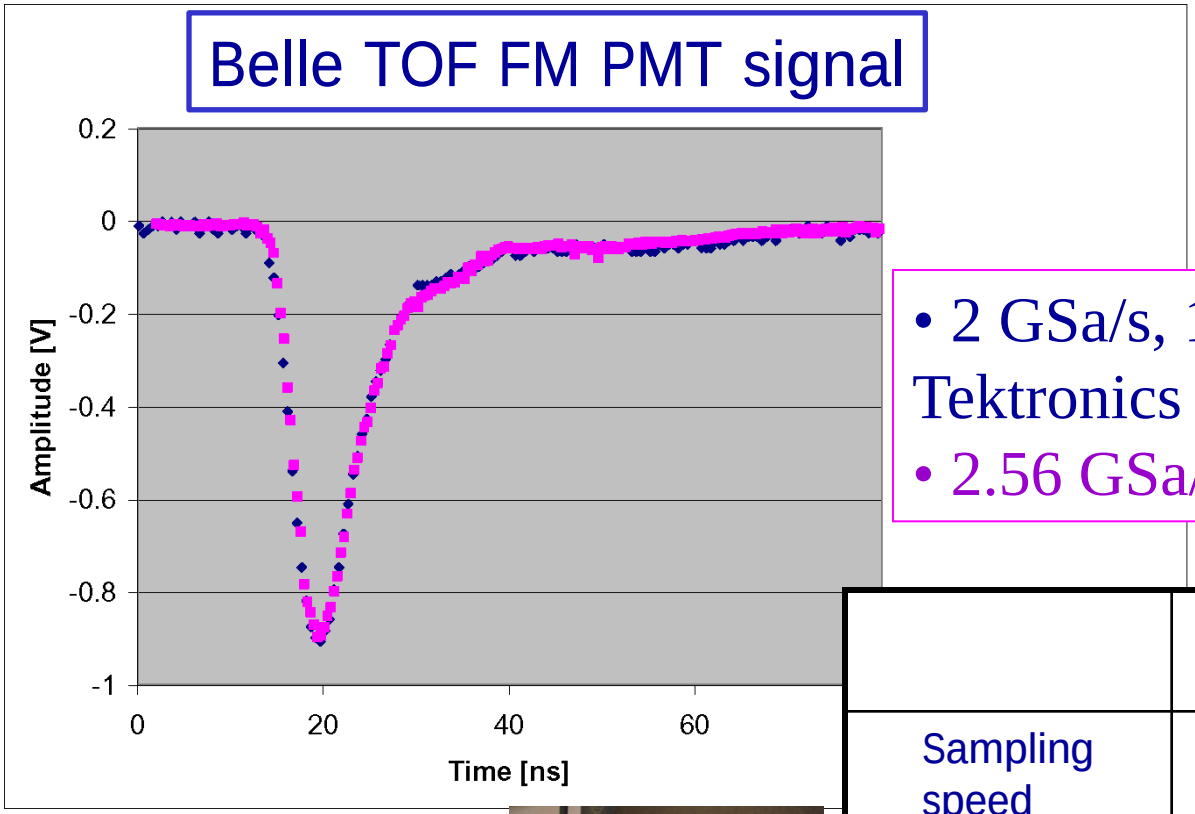
DRS4,
MEG Experiment

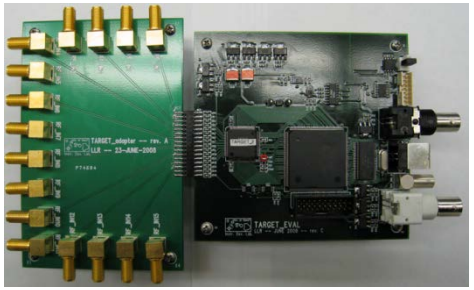
SAM,
H.E.S.S.-II





An Easily understood Selling Point

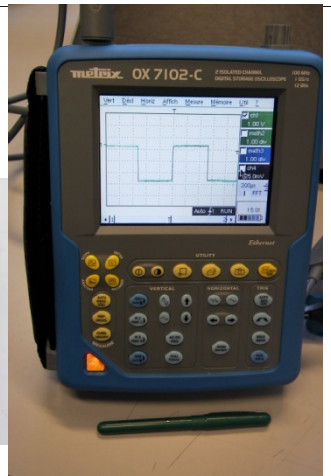




- 2 GSa/s, 1GHz ABW Tektronics Scope
- 2.56 GSa/s LAB

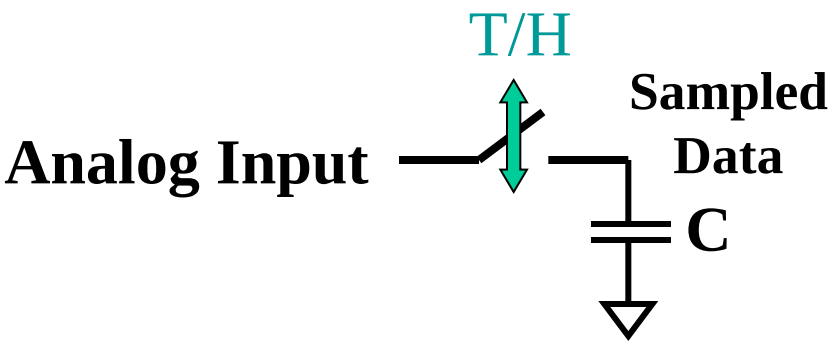
	WFS ASIC	Commercial
Sampling speed	0.1-6 GSa/s	2 GSa/s
Bits/ENOBs	16/9-13+	8/7.4
Power/Chan.	<= 0.05W	Few W
Cost/Ch.	< $10 (vol)	> 100$

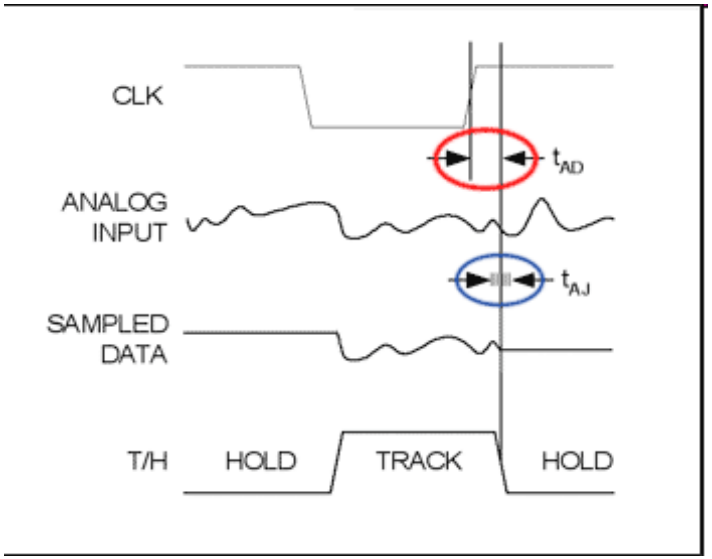
"oscilloscope on a chip"



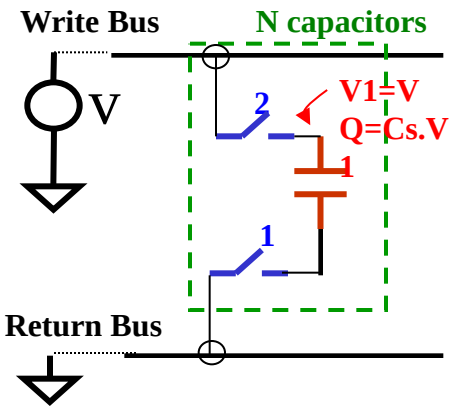
Underlying Technology

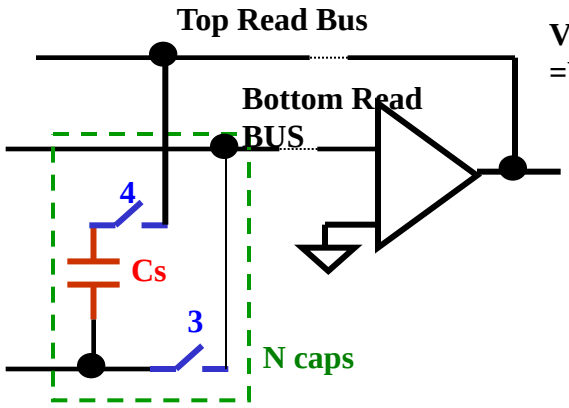
- Track and Hold (T/H)





- Pipelined storage = array of T/H elements, with output buffering

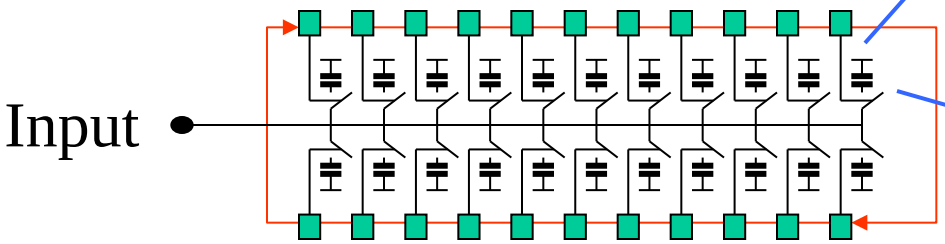


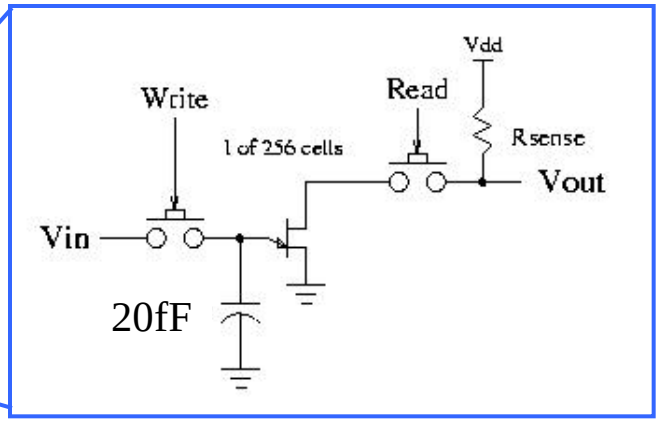


Vout=A / (1+A) * Q/Cs
=V1 * A/(1+A)

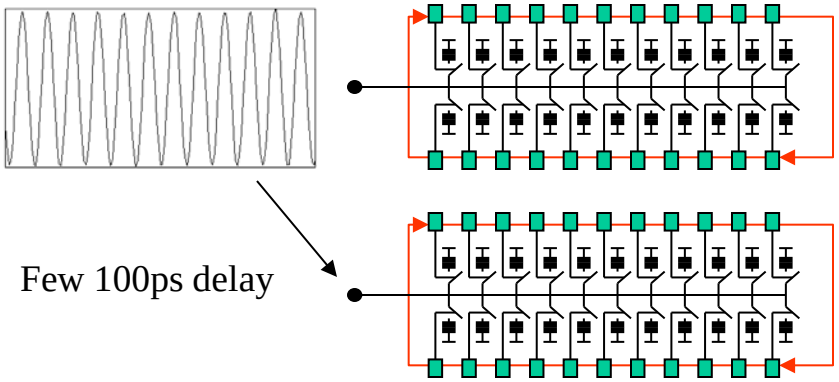
Switched Capacitor Array Sampling

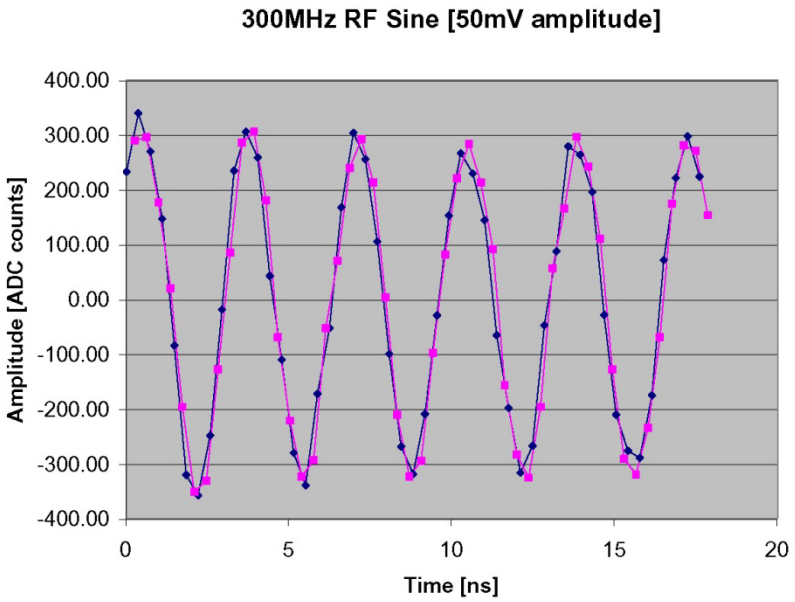
- Write pointer is ~few switches closed @ once



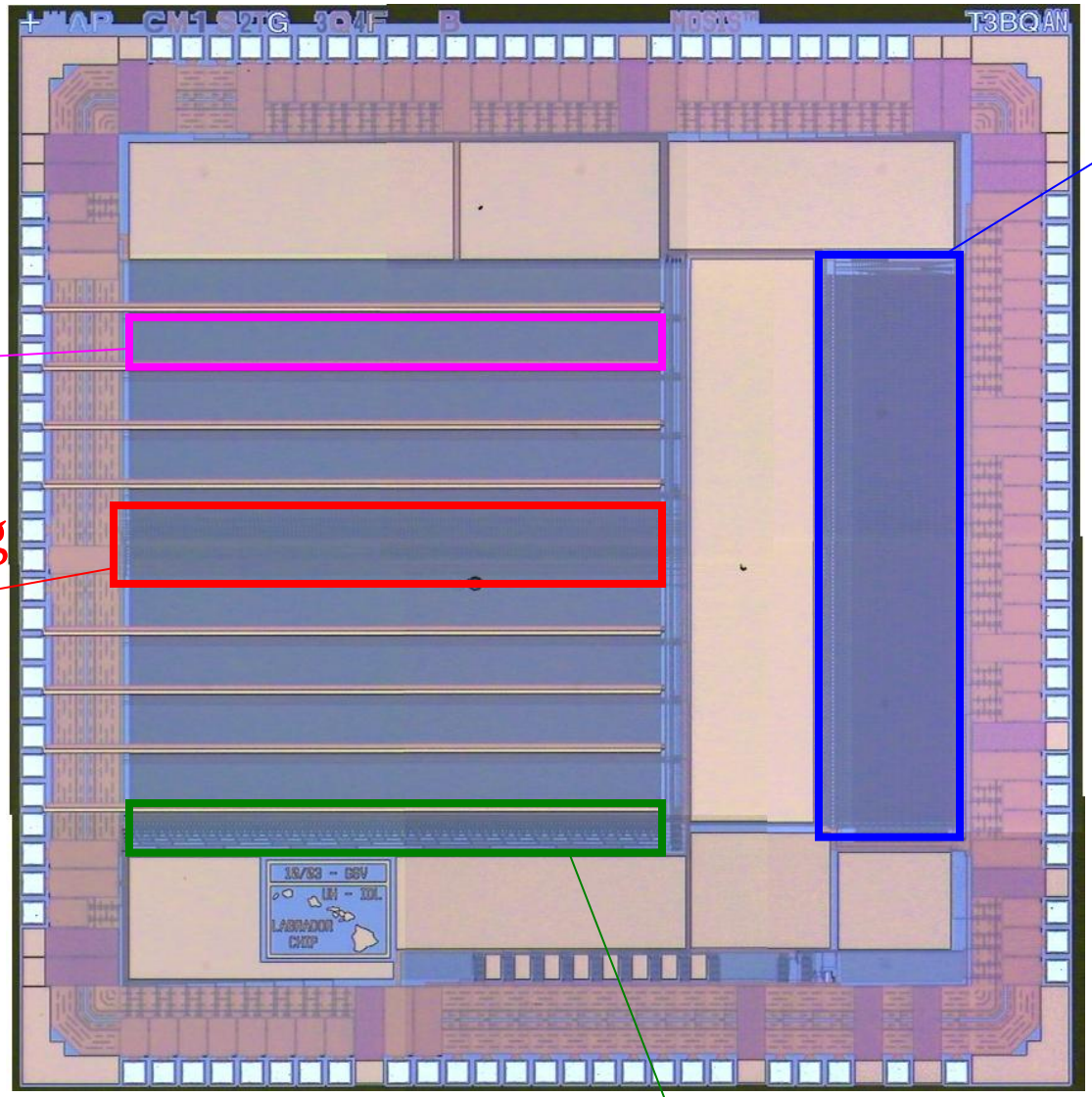


Tiny charge: 1mV ~ 100e$^-$





Basic Functional components

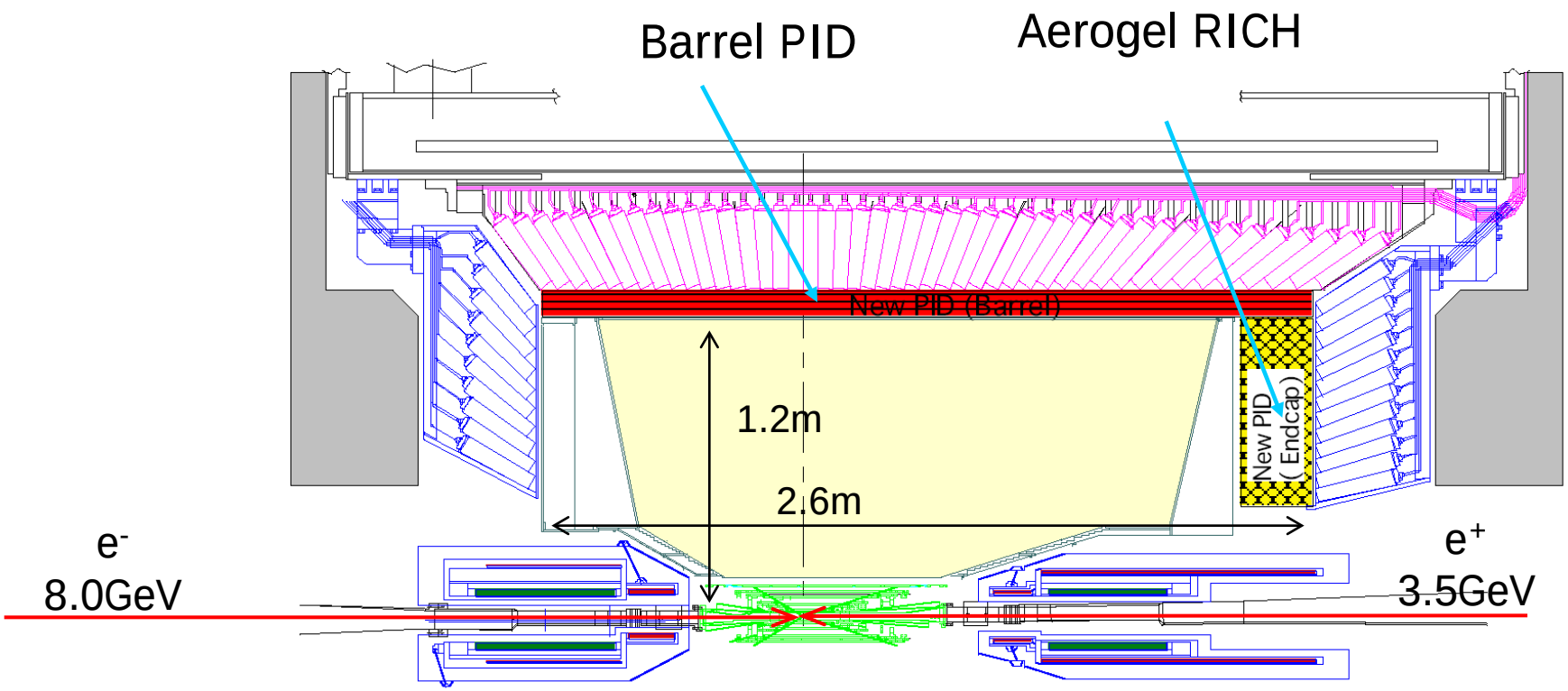


Upgraded Belle detector

- PID (π/K) detectors
- Inside current calorimeter
- Use less material and allow more tracking volume

→ Available geometry defines form factor

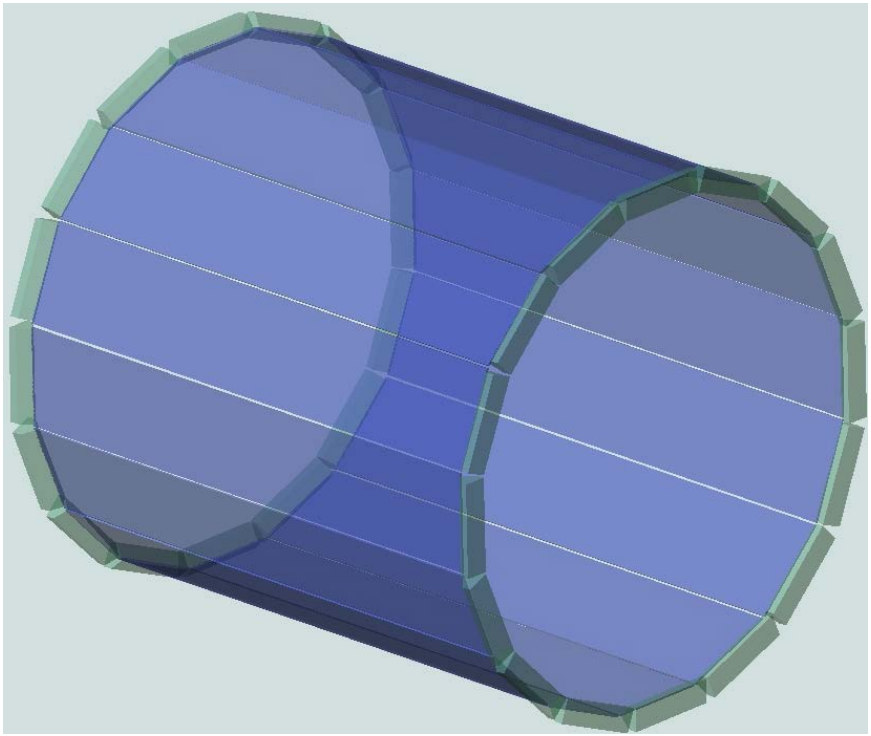
-

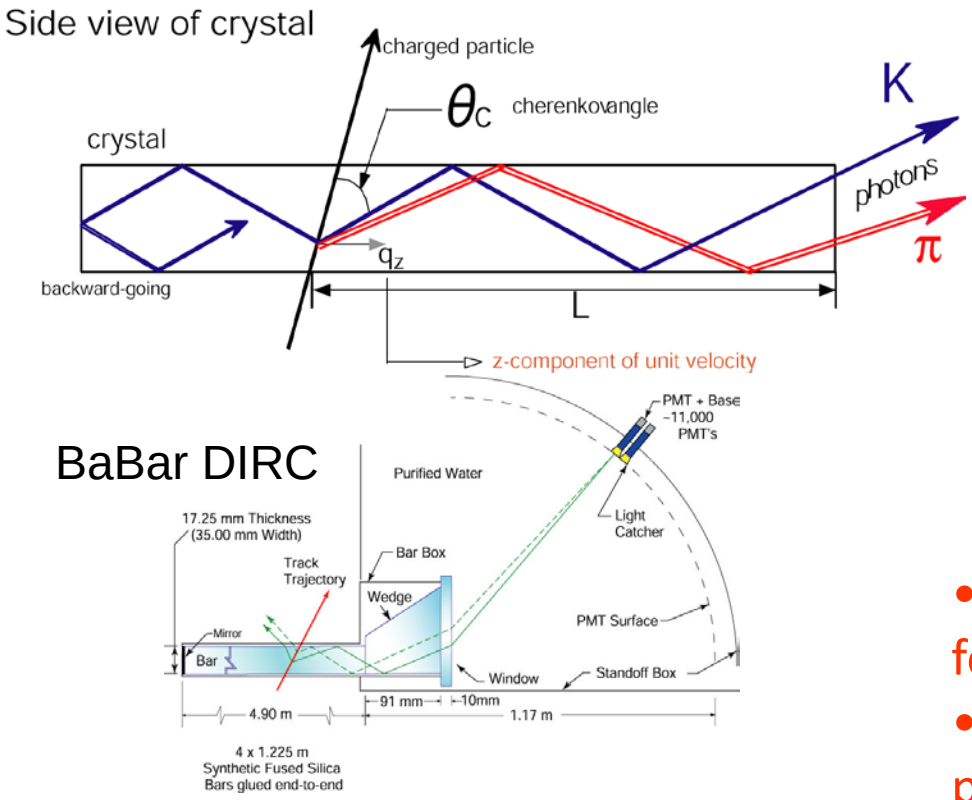


imaging TOP (iTOP)

Concept: Use best of both TOP (timing) and DIRC while fit in Belle PID envelope

NIM A623 (2010) 297-299.



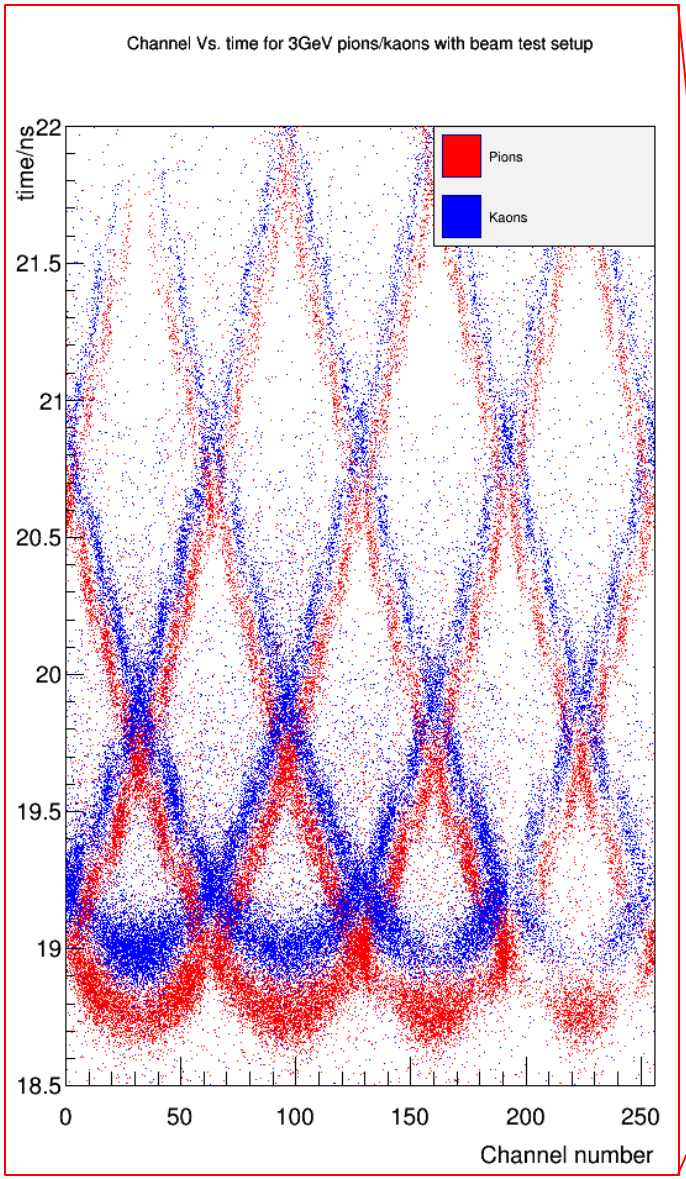


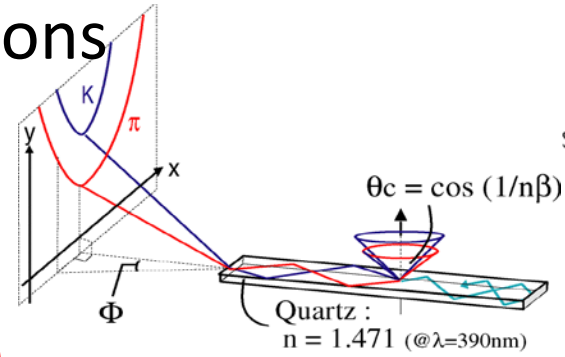
Use wide bars like proposed TOP counter

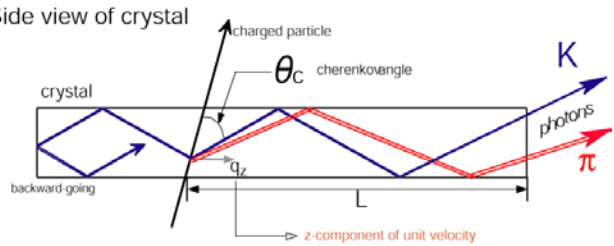
- Use new, high-performance MCP-PMTs for sub-50ps single p.e. TTS
- Use simultaneous T, θc [measured-predicted] for maximum K/π separation
- Optimize pixel size

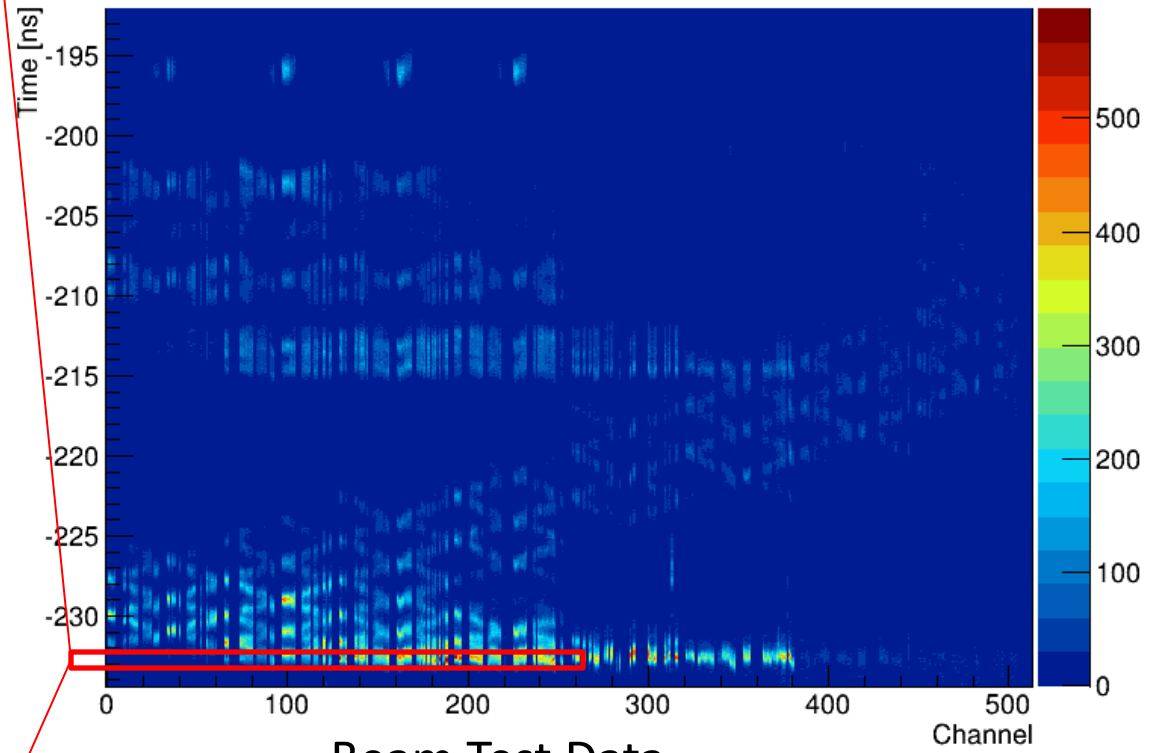
iTOP relativistic velocity

- Space-time correlations







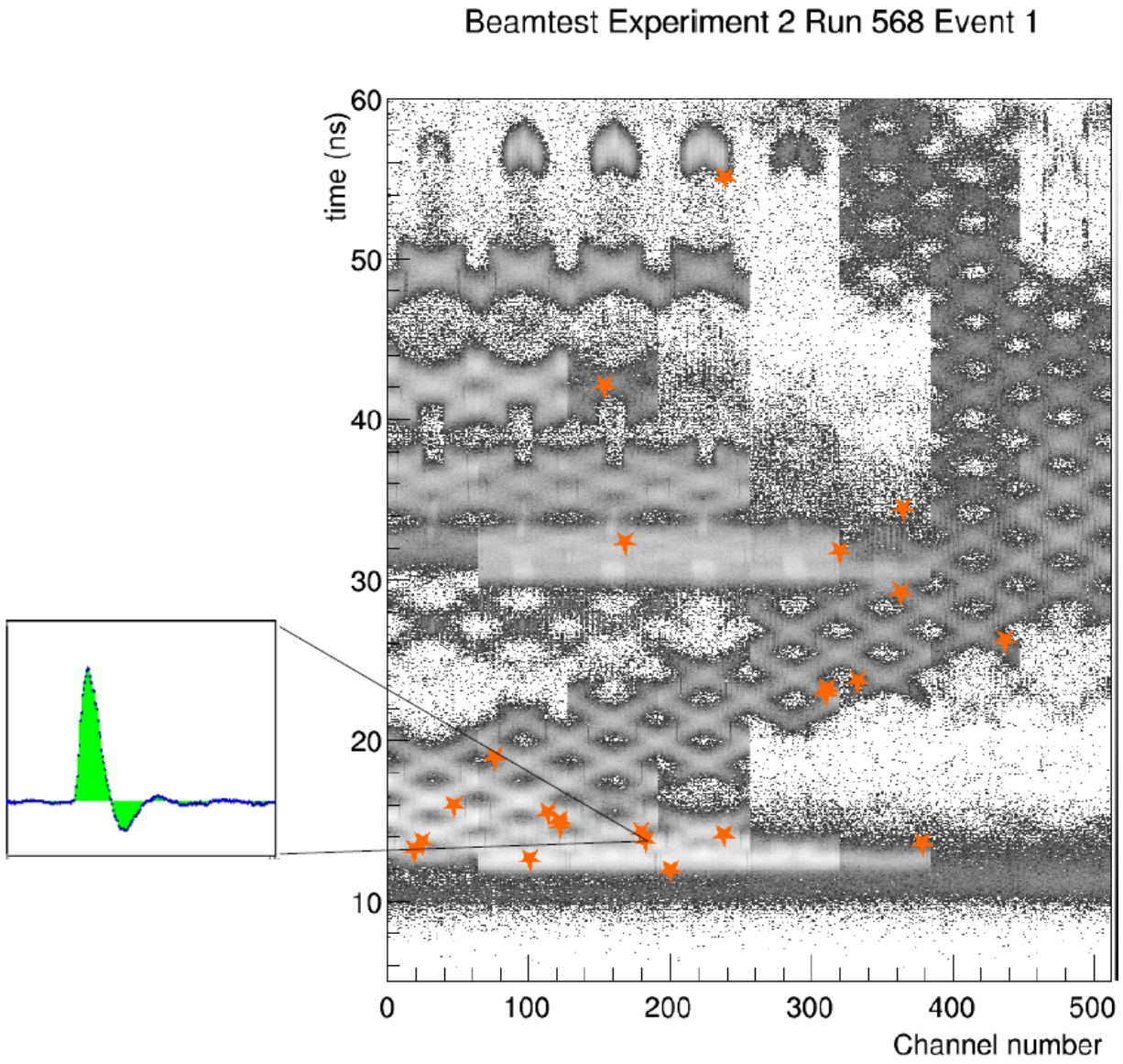


Beam Test Data

These are cumulative distributions

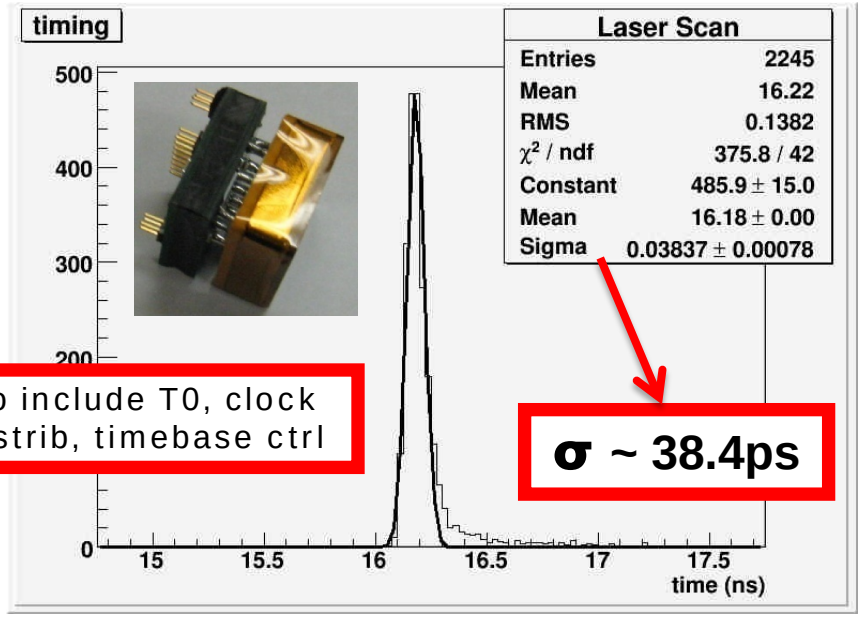
Actual PID is event-by-event

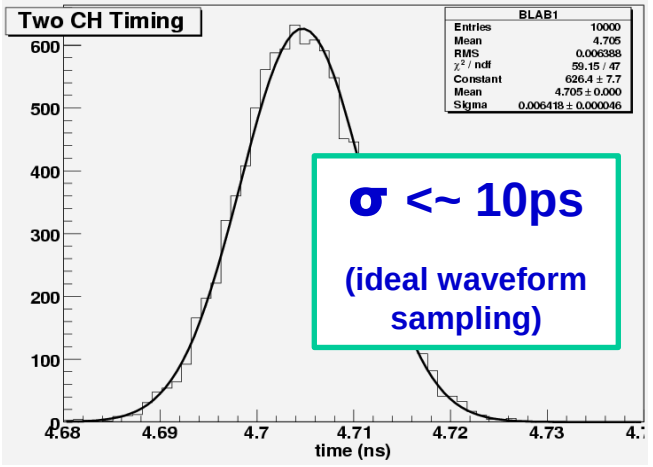
- Test most probable distribution



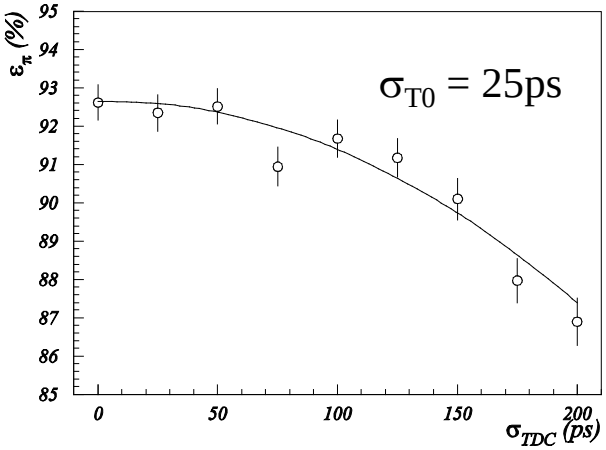
Single photon detection for TOP

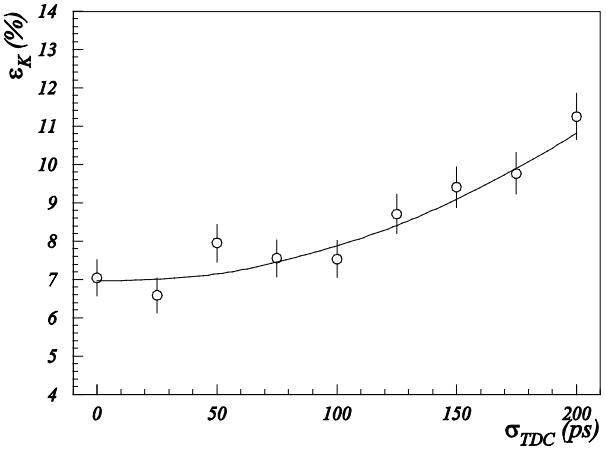
- Single photon timing for MCP-PMTs





NIM **A602** (2009) 438



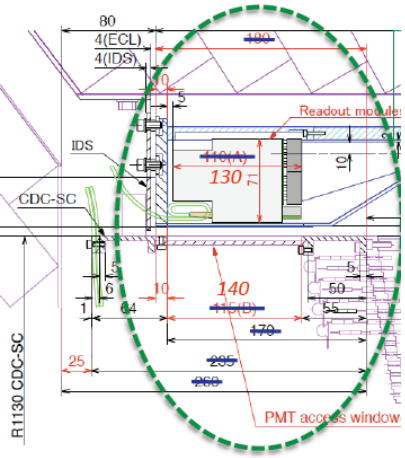


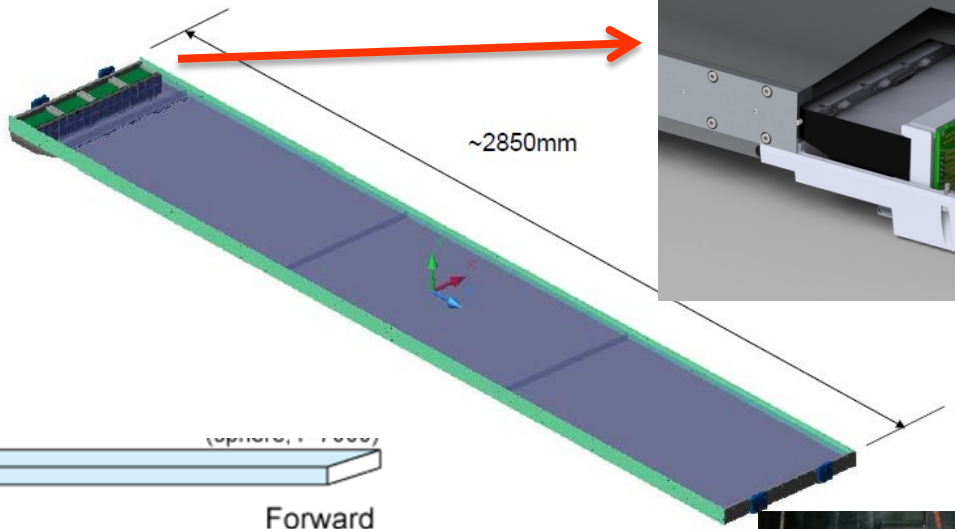
σ <~ 50ps target

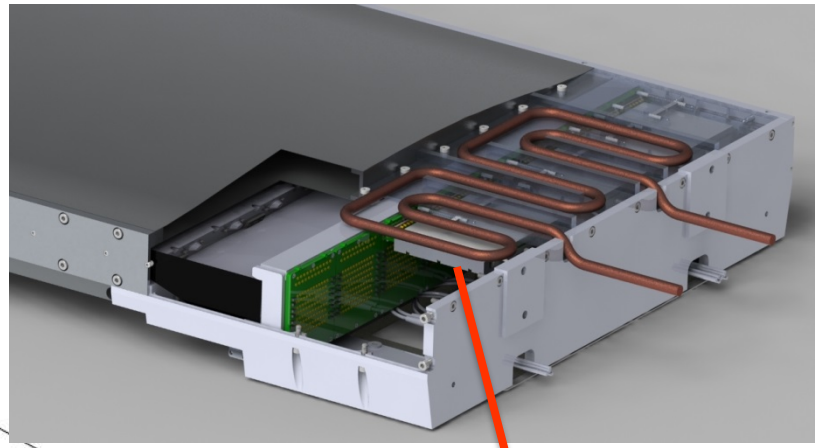
NOTE: this is single-photon timing, **not** event start-time "T_0"

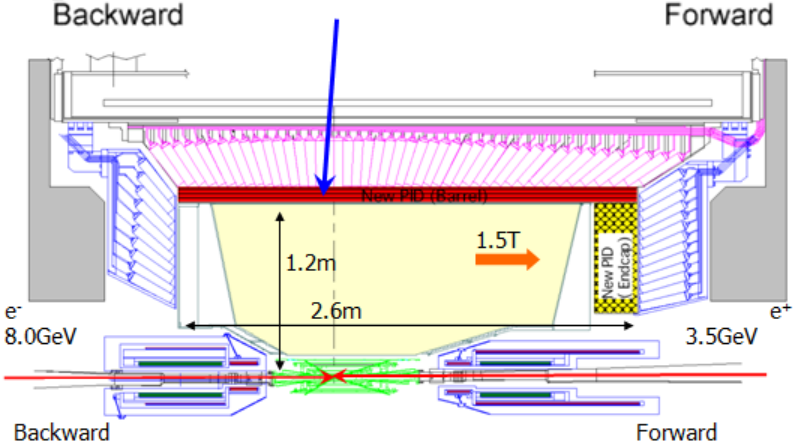
Highly integrated services

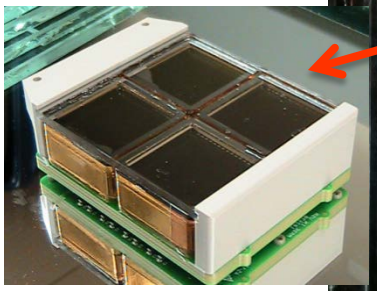
- A severely constrained space

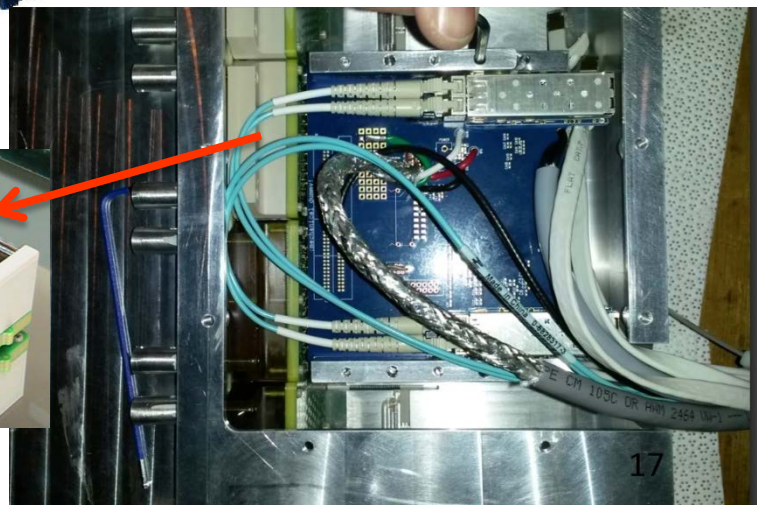








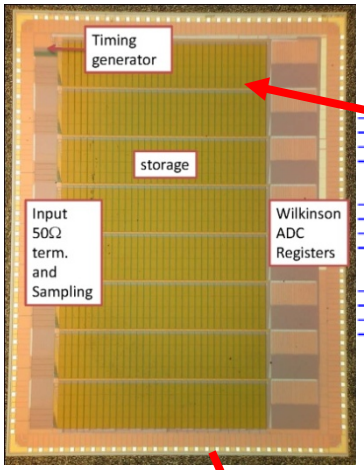


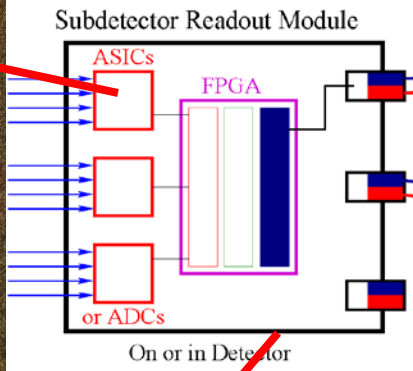


imaging TOP Readout (FDIRC proto)

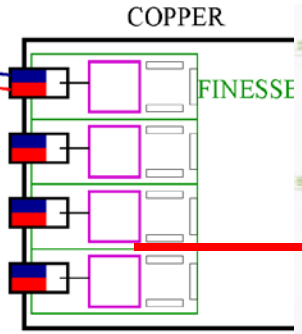
Waveform sampling ASIC

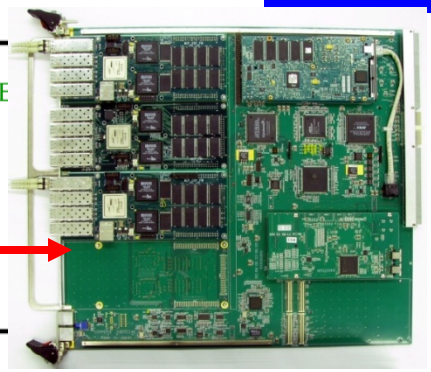
64 DAQ fiber transceivers



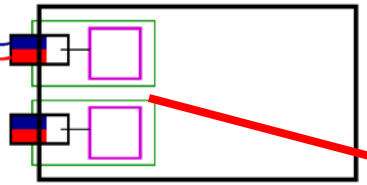


Giga-bit Fiber Transceiver Links





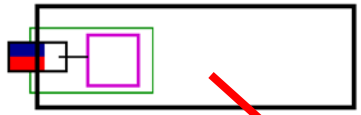
64 FINESSE
16 COPPER



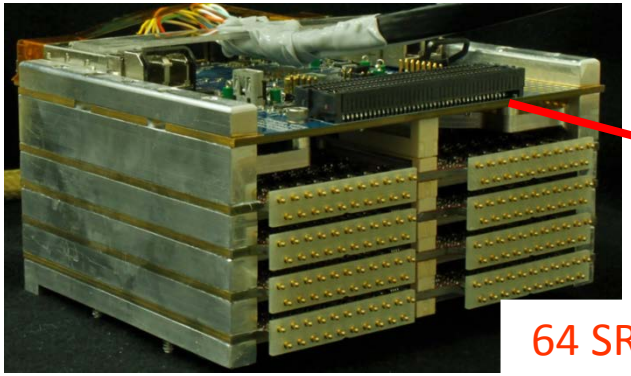
2x UT3 Trigger modules

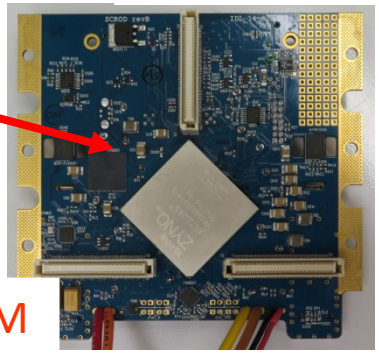
FPGA firmware consists of 3 parts:
1) ASIC/ADC driver (common)
2) Trigger feature extract (subdet. specific)
3) Unified DAQ transport protocol

8k channels
1k 8-ch. ASICs
64 "board stacks"



Low-jitter clock





64 SRM

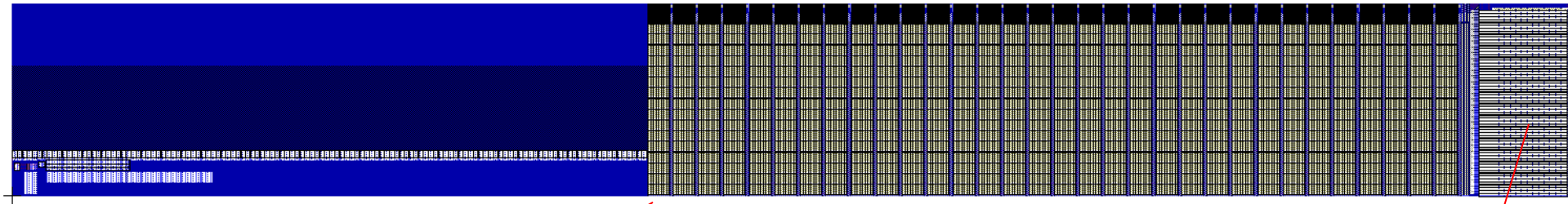
Clock, trigger, programming module (FTSW)

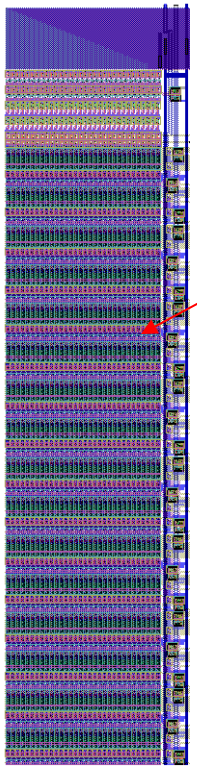
8 FTSW

IRSX Single Channel

- Sampling: 128 (2x 64) separate transfer lanes

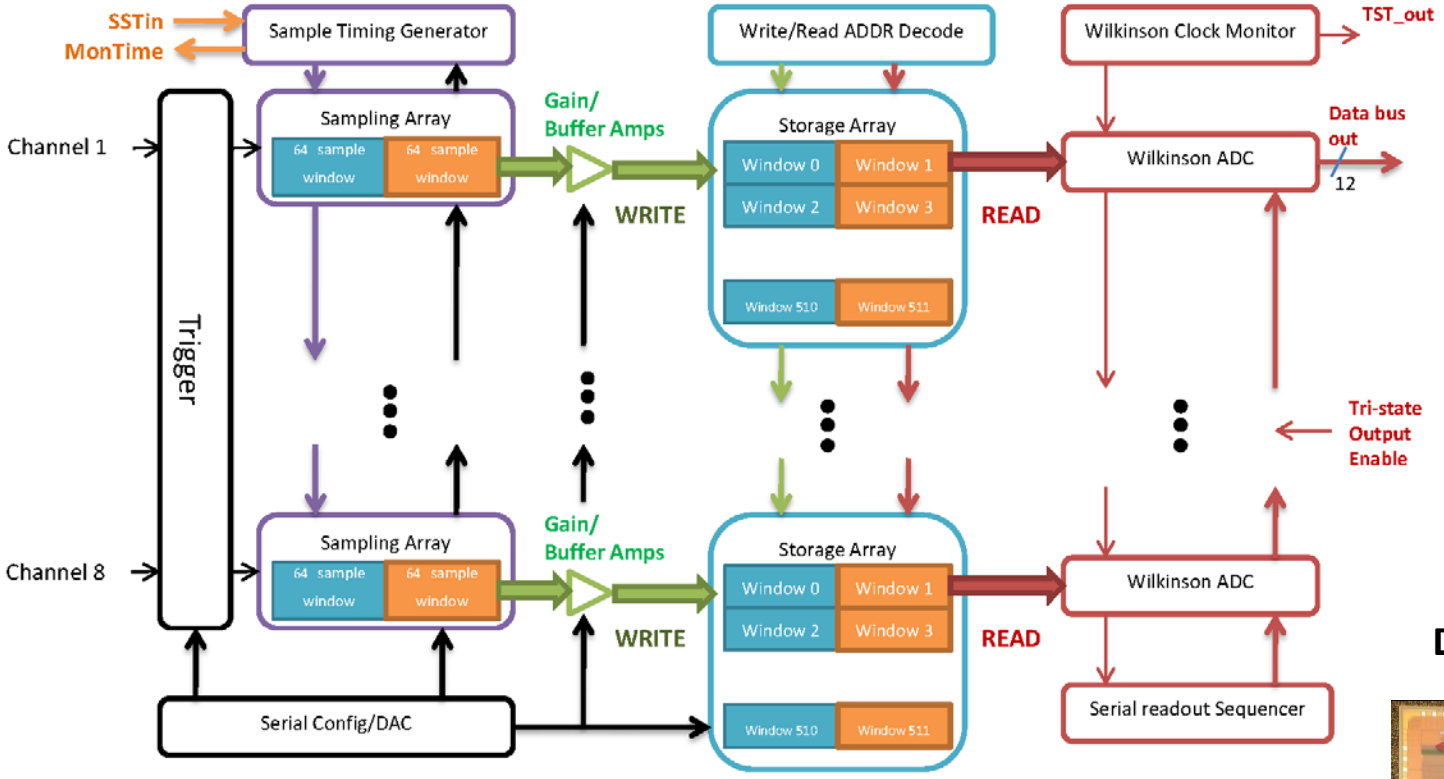
Recording in one set 64, transferring other (“ping-pong”)





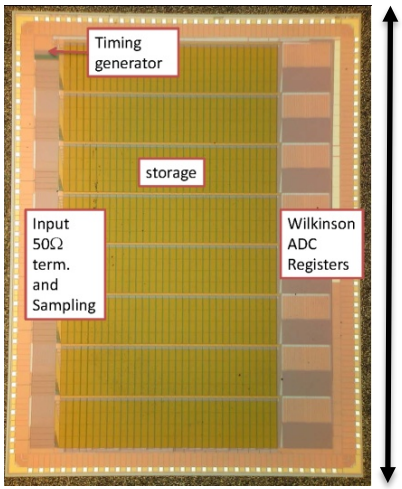
- Concurrent Writing/Reading
- Only 128 timing constants
- Storage: 64 x 512 (512 = 8 * 64)
- Wilkinson (64x1): was (32x2)
- 64 conv/channel

IRSX ASIC Overview



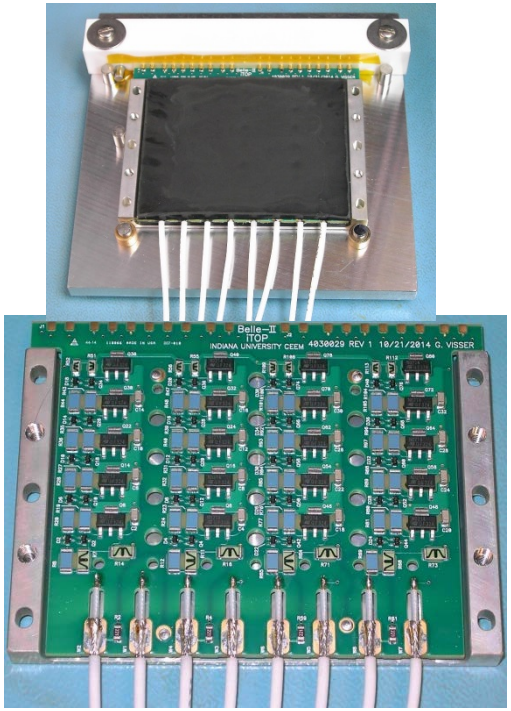
- 8 channels per chip @ 2.8 GSa/s
- Samples stored, 12-bit digitized in groups of 64
- 32k samples per channel (11.6us at 2.8GSa/s)
- Compact ASICs implementation:
  - Trigger comparator and thresholding on chip
  - On chip ADC
  - Multi-hit buffering

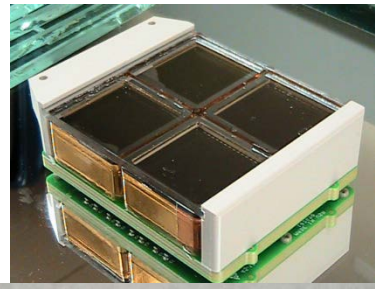
Die Photograph

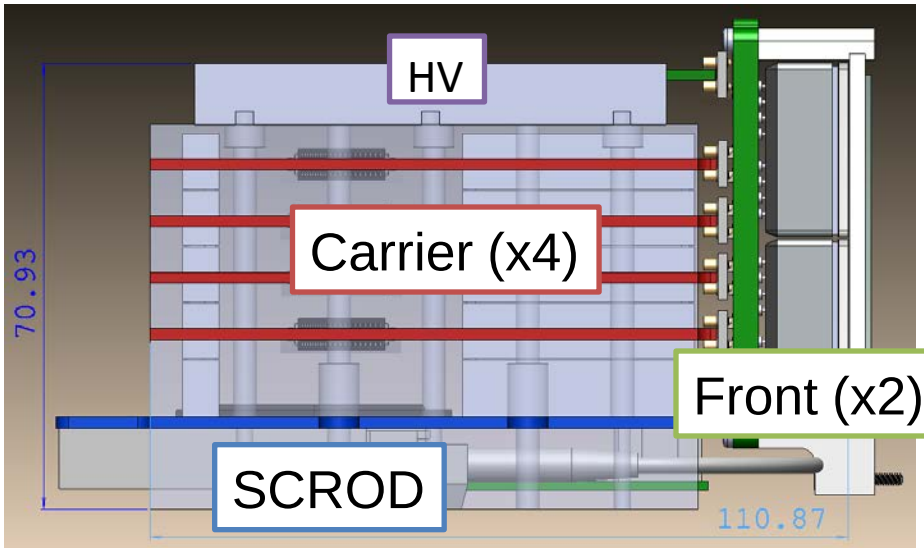


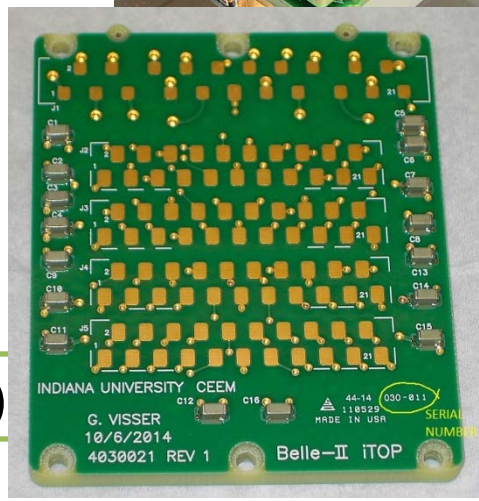
iTOP Readout “boardstack”

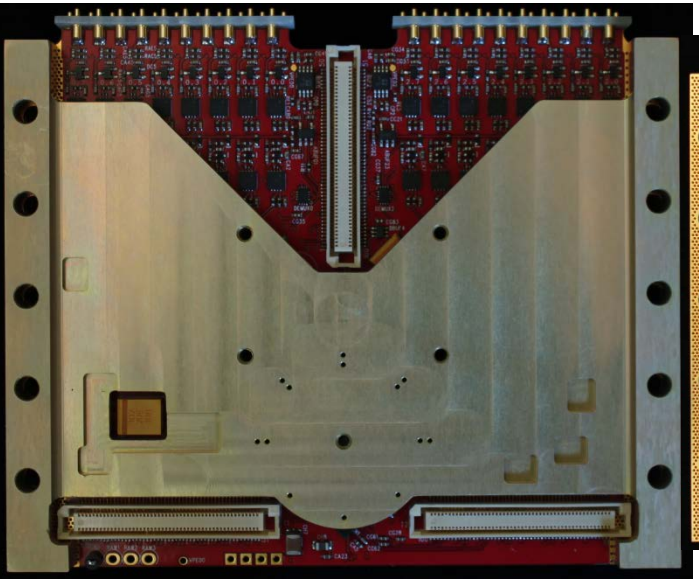
(1 of 4 per TOP Module)

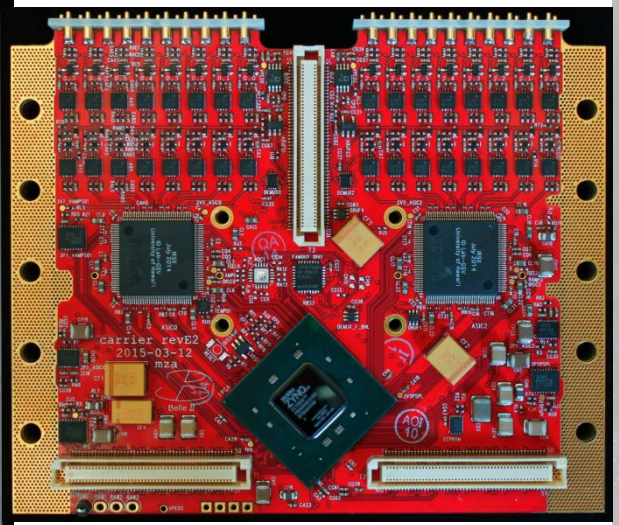




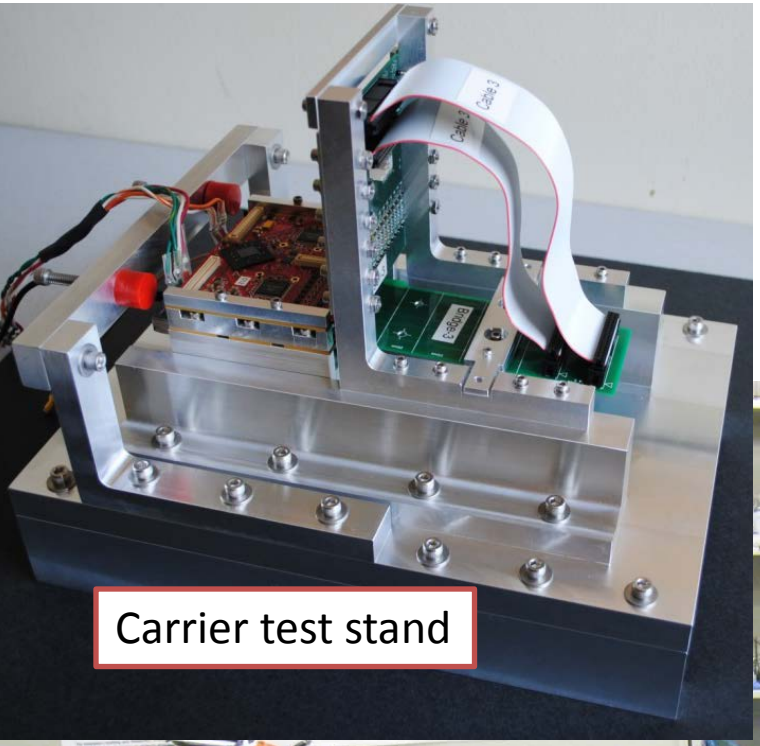




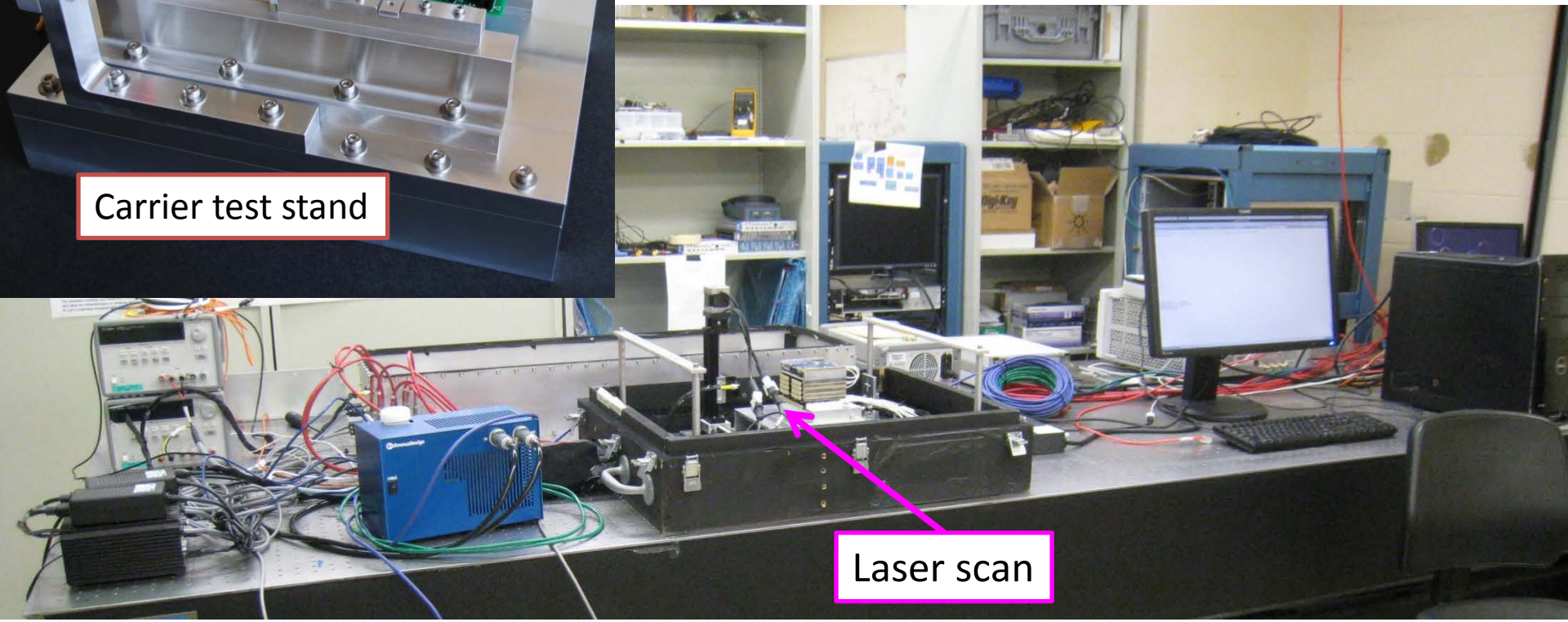




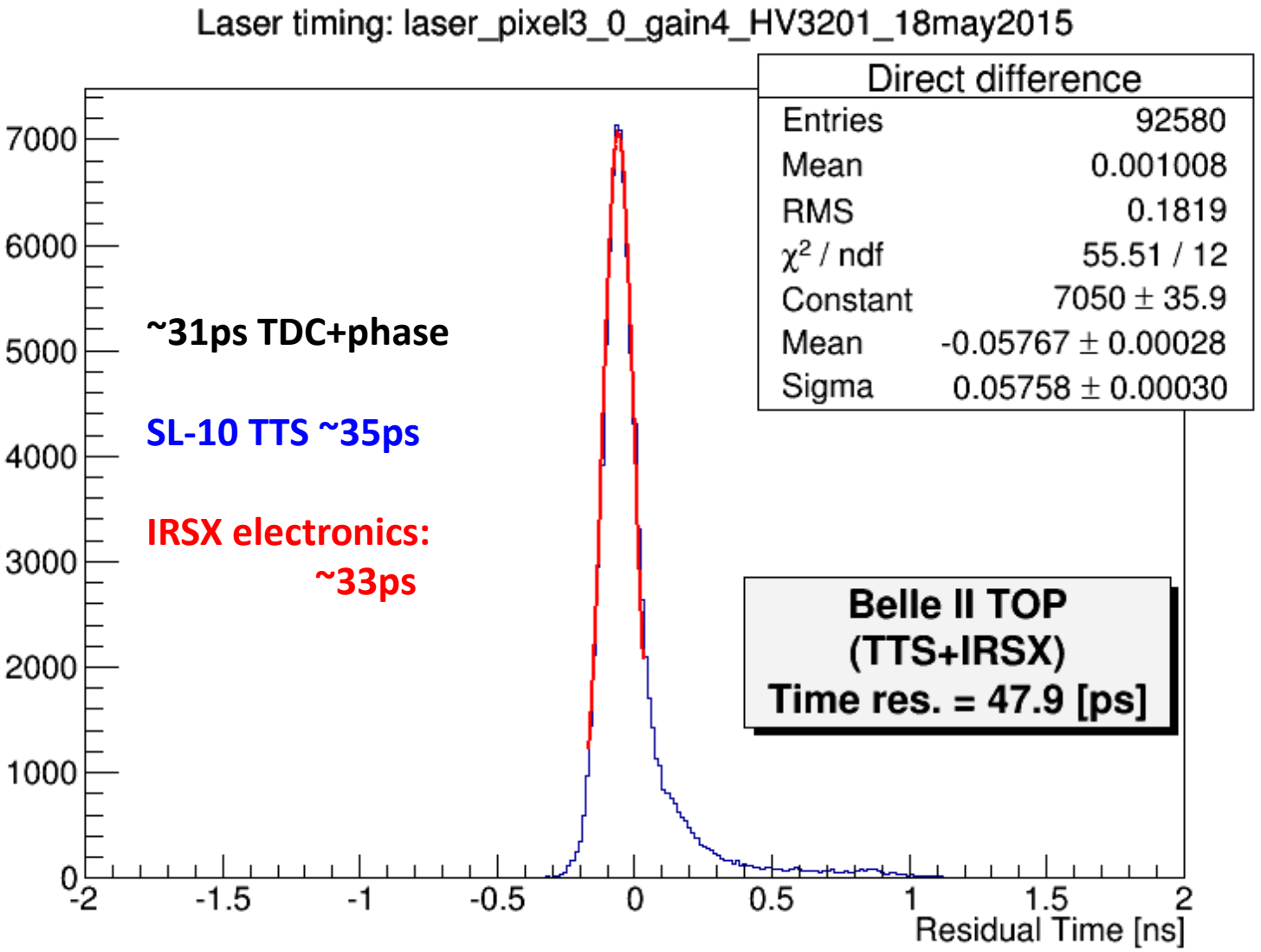
iTOP Readout Production Testing



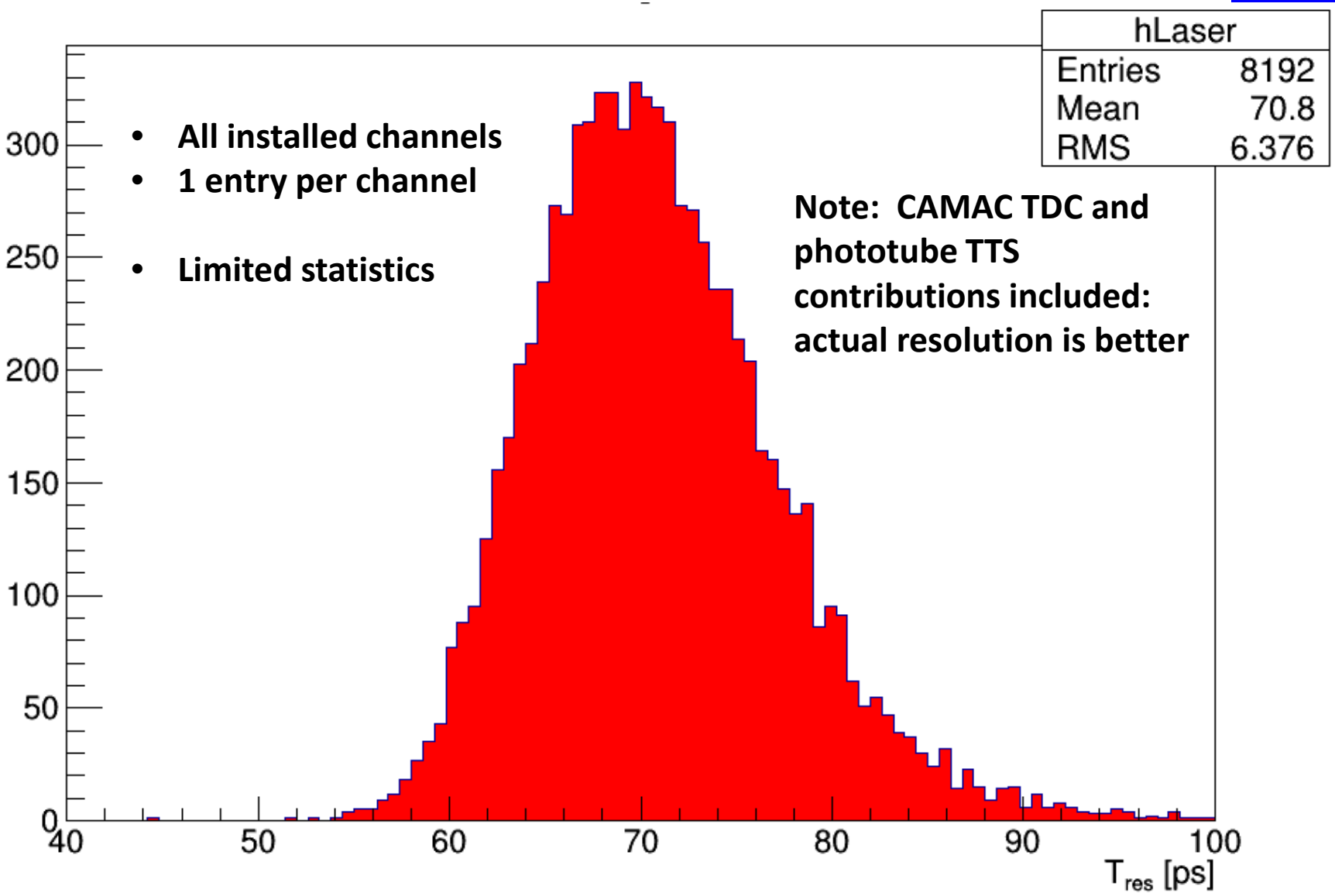
- **2x Carrier test stations at South Carolina, 1x backup in Hawaii**
- **Laser test stand Hawaii**
- **SCROD test stand in Pittsburgh**
- **Firmware test at PNNL**



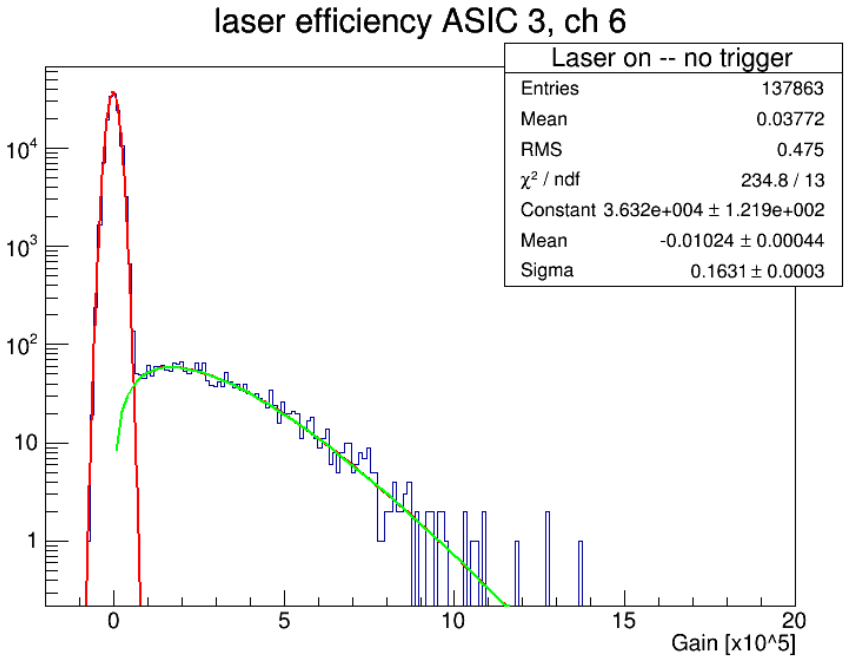
Production single photon testing

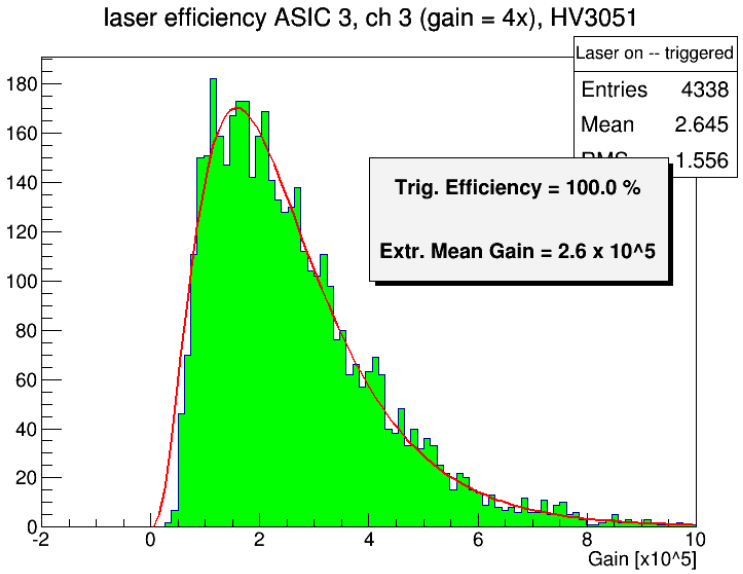


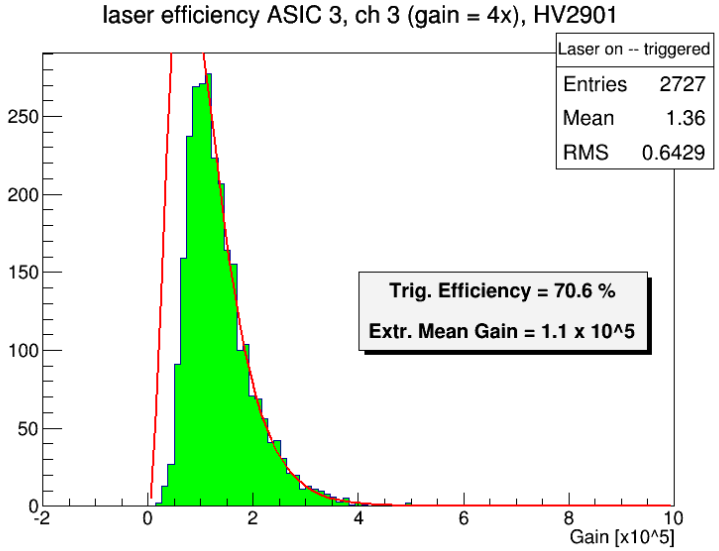
Production – initial single photon timing

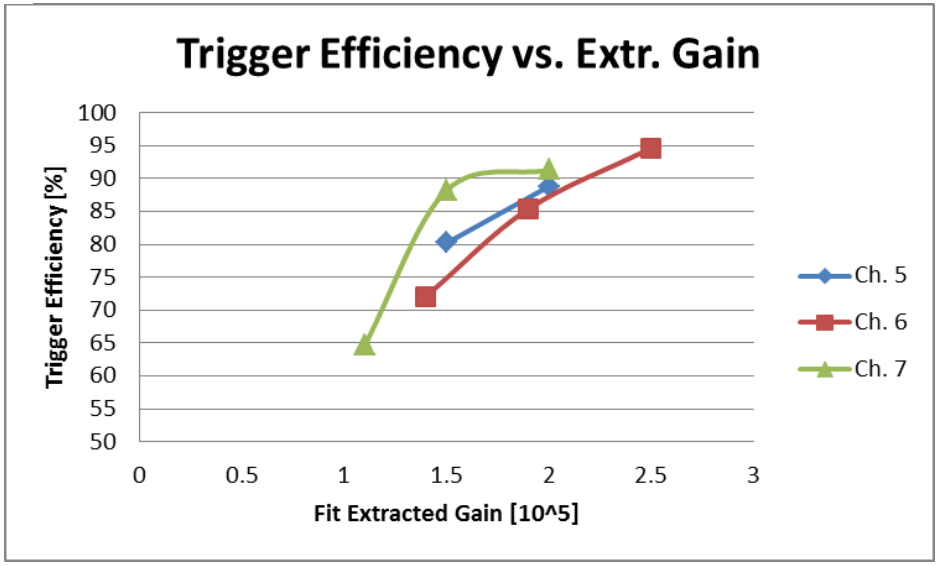


If single photon, why bother?

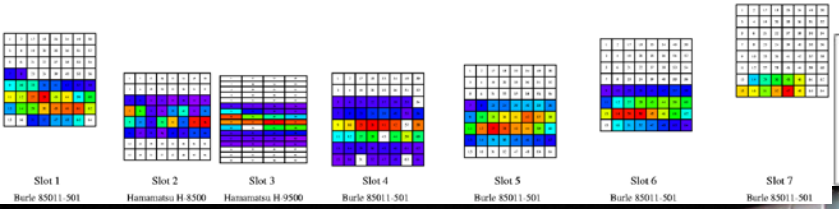


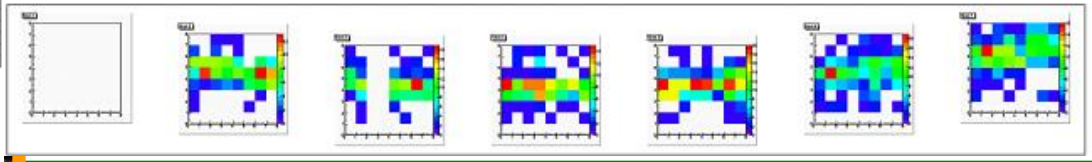


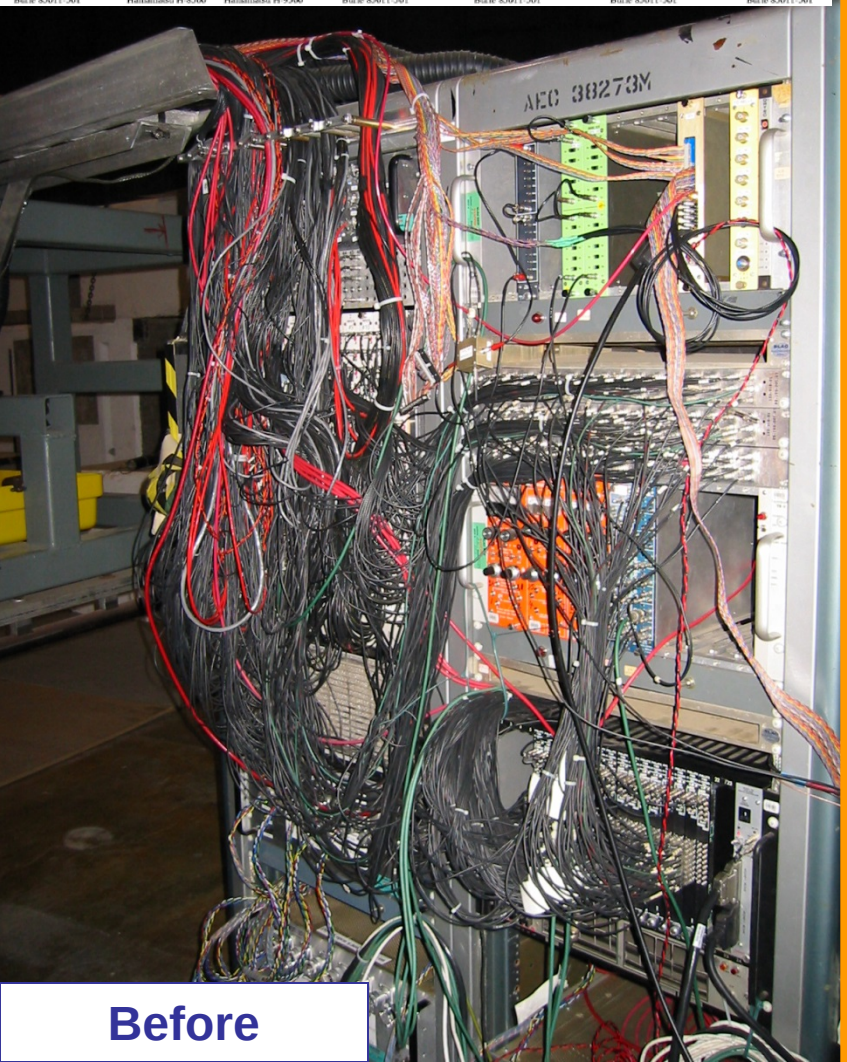




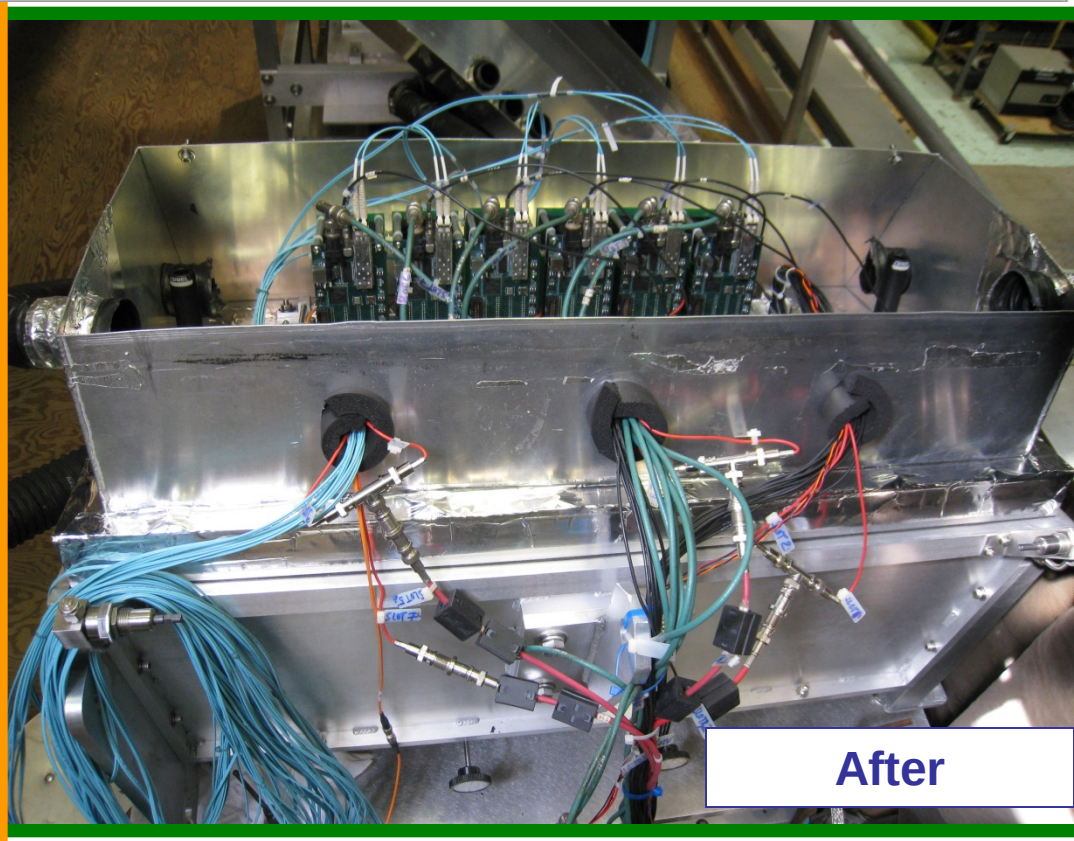
FDIRC Experience







Before



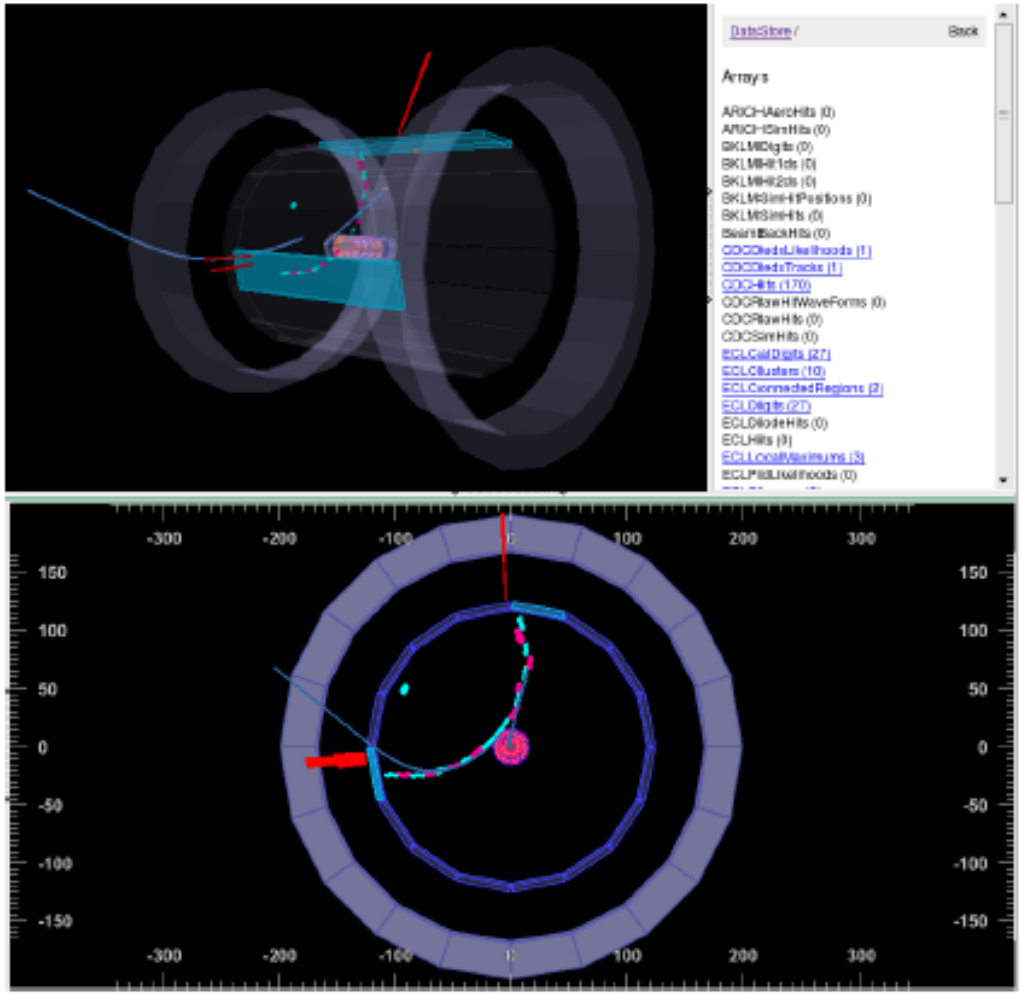
After

“Is that it?!?”

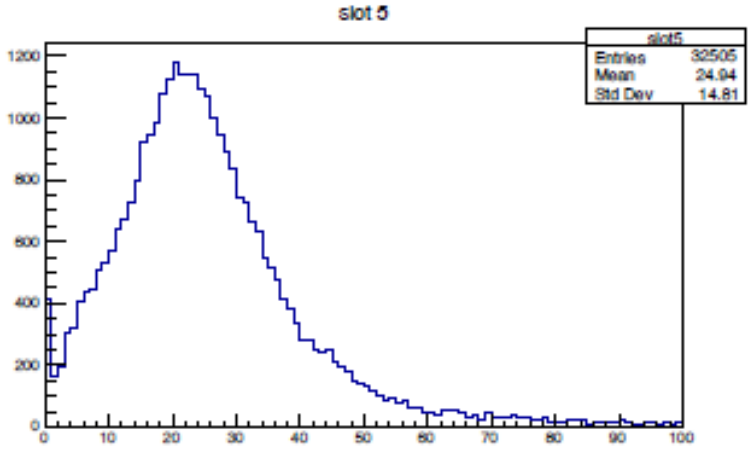
-Matt McCulloch (surprise at how few cables were used in the upgrade)

Focus now

Global Cosmic Ray Test



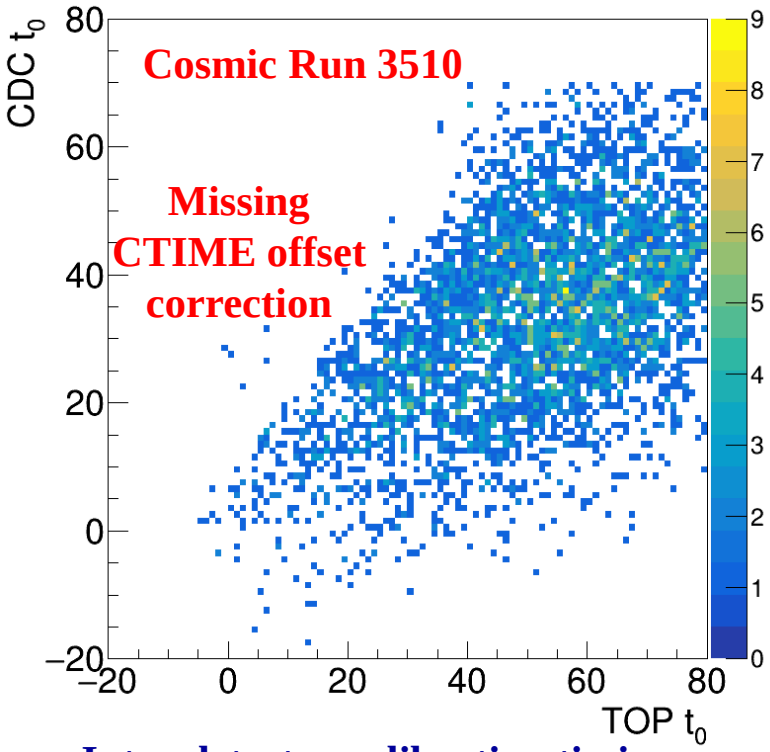
- Global cosmic ray data taking started since July 3, 2017
- Outer detectors including TOP joined the data taking
- Rough number of photon hits per events agrees with MC
- More detailed analyses are ongoing



Calibrations Ongoing

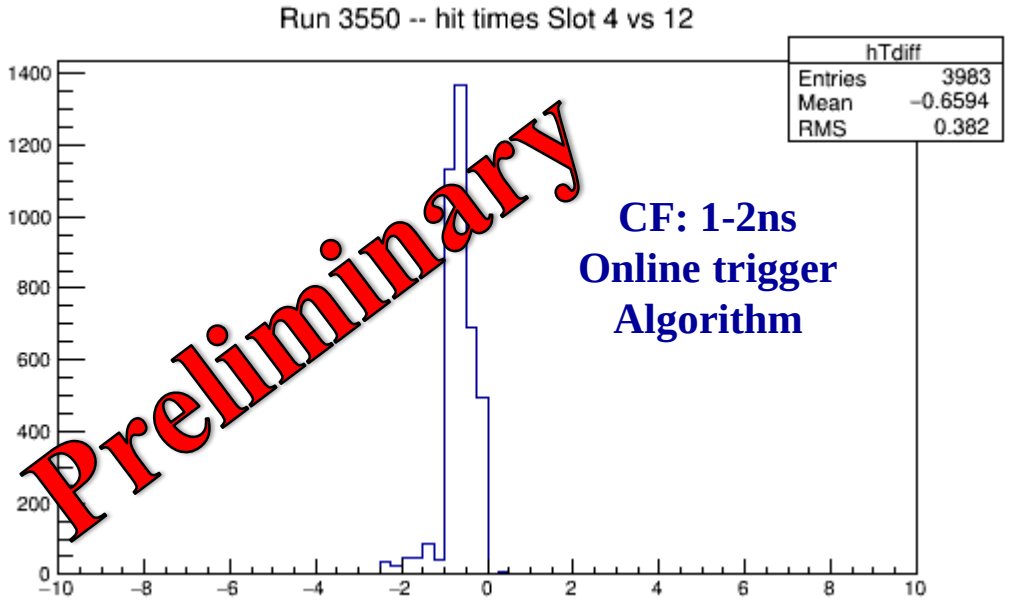
- Sampling timebase (inject reference pulse pair)
- Channel-channel alignment (laser calibration)
- Module-module alignment (readout aligned to SuperKEKB clock)
- Subdetector (x,y,z), T alignment (global runs July, Aug 1.5T field)

First combined data taking



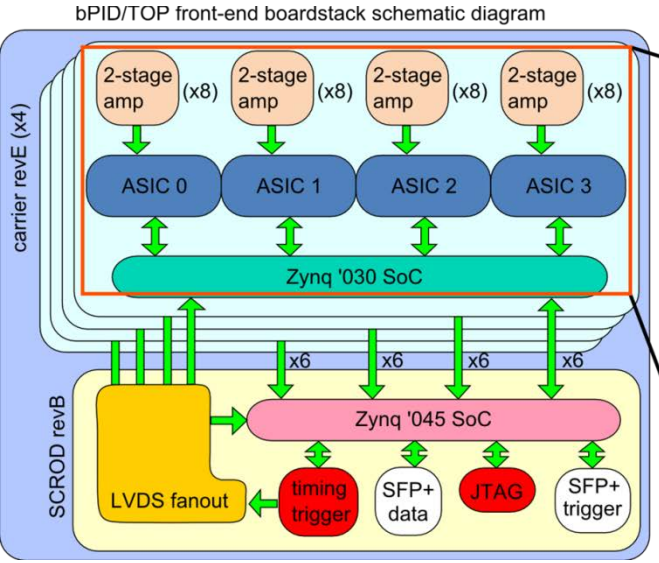
Inter-detector calibration timing

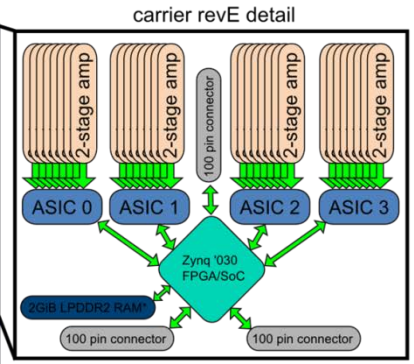
Versus stand-alone



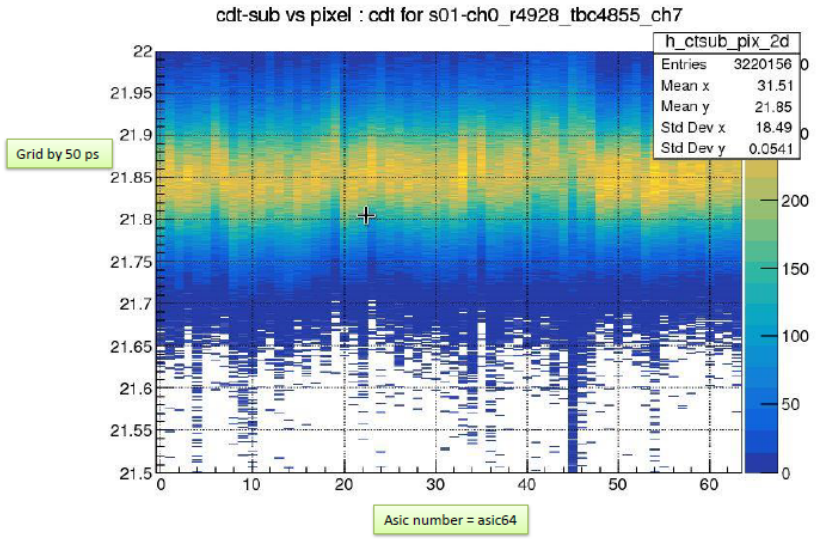
TOP only: <T_4> - <T_12> (top – bottom)
No detailed alignment

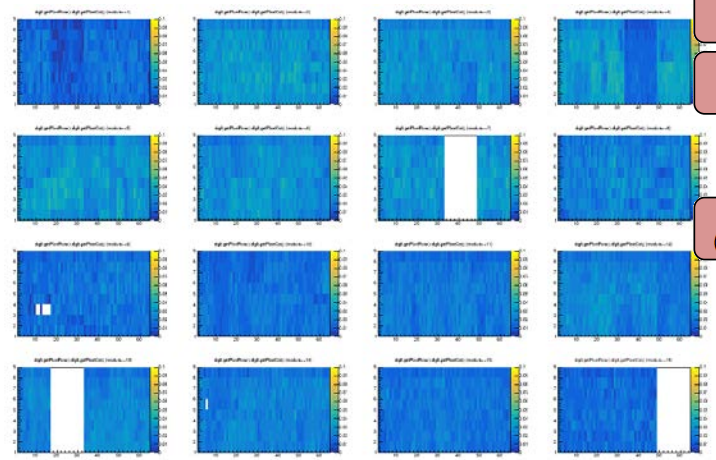
Biggest challenge: Firmware complexity

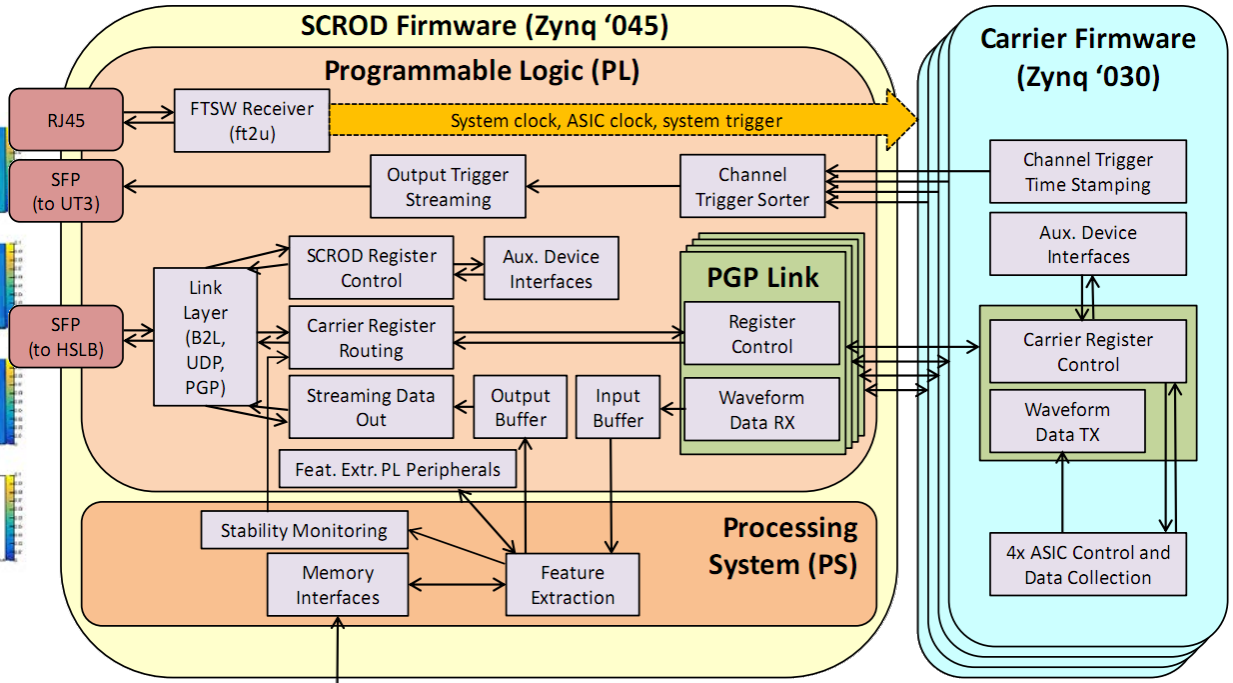




in addition, on the board, there are:
11 voltage regulators
voltage and current monitoring for all regulators
power supply sequencing logic
calibration signal amplification and fanout
automatic fallover wiring to close JTAG chain
temperature sensor (i2c)
EEPROM (i2c)

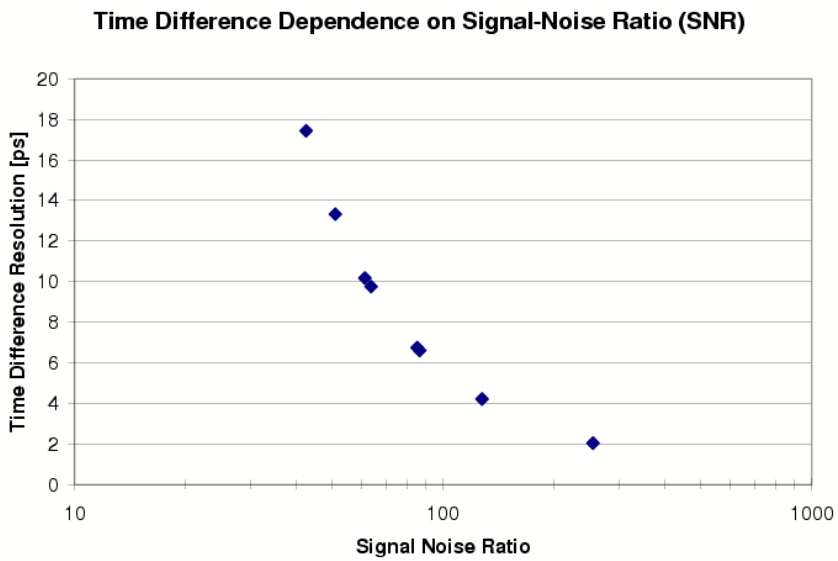






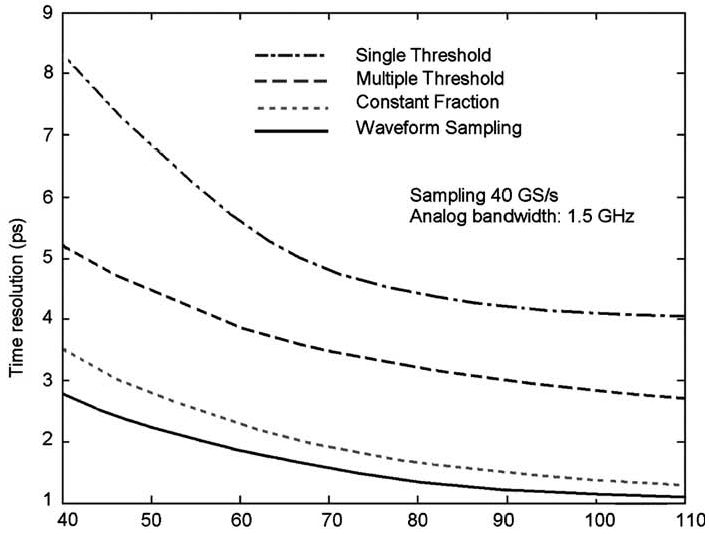
Technology has room to improve

1GHz analog bandwidth, 5GSa/s



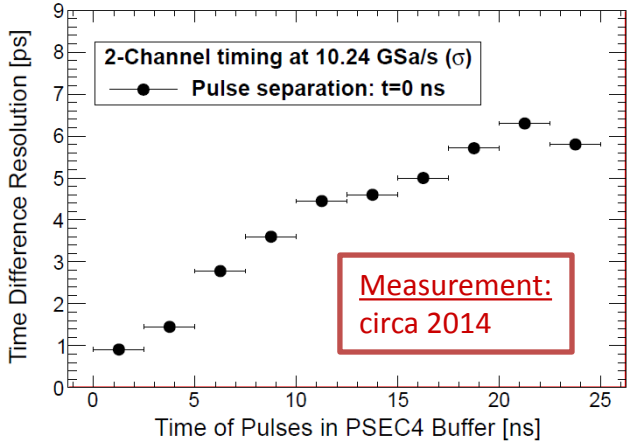
G. Varner and L. Ruckman
NIM A**602 (2009) 438-445**.

Simulation includes detector response



J-F Genat, G. Varner, F. Tang, H. Frisch
NIM A**607 (2009) 387-393**.

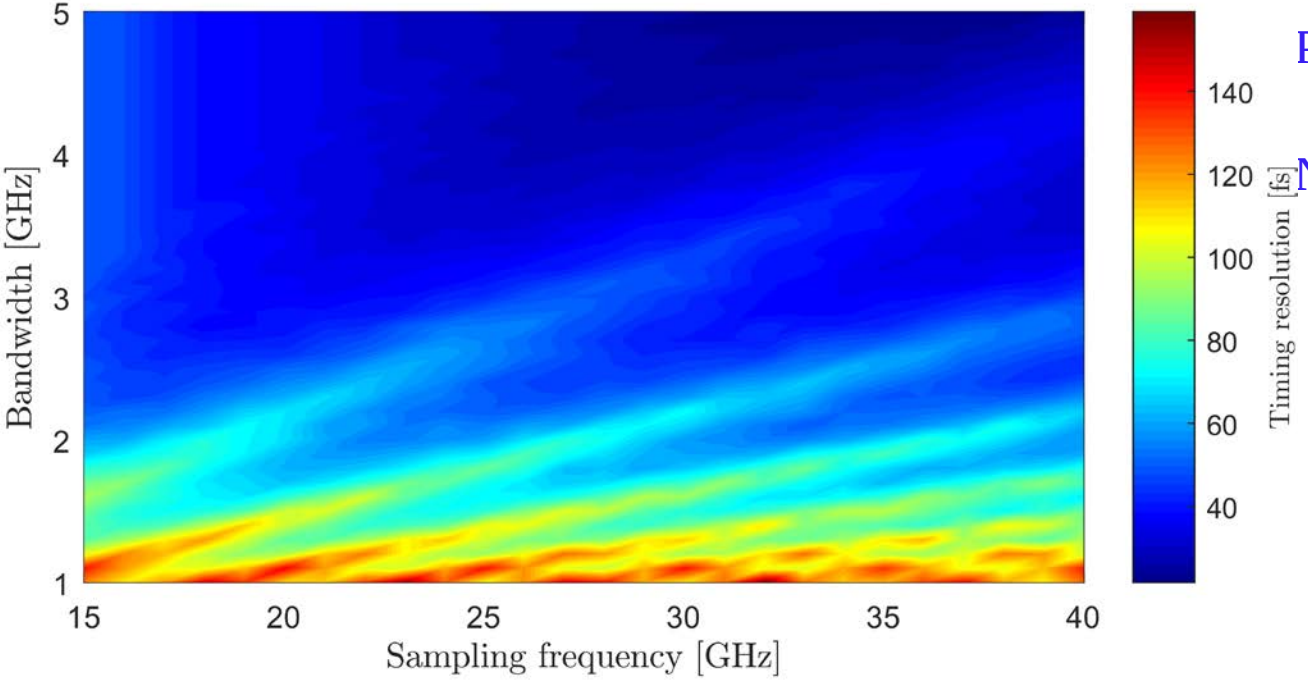
E. Oberla, J-F Genat,
H. Grabas, H. Frisch,
K. Nishimura, G. Varner
NIM A**735 (2014) 452-461**.



Extending to 1ps and lower, with advanced calibration techniques

Now pushing to the femtosecond regime

Pushing sampling speed and analog bandwidth



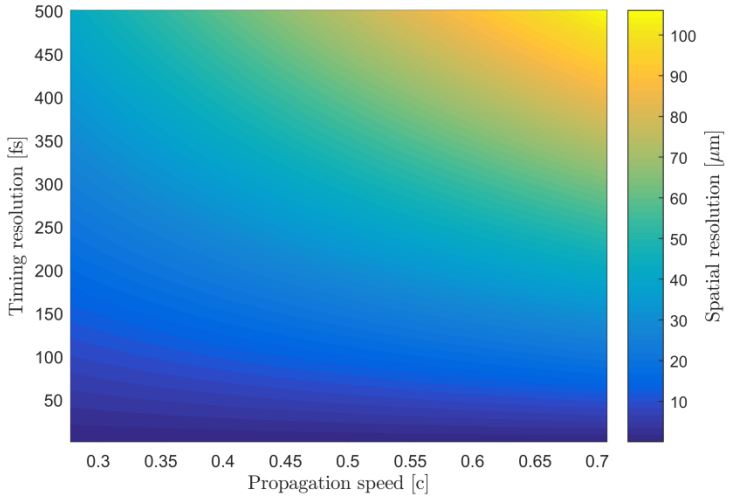
P. Orel, G. Varner and P. Niknejadi

NIM A**857 (2017) 31-41**.

And pushing the **space-time limit**
(new type of PID or DIRC devices?)

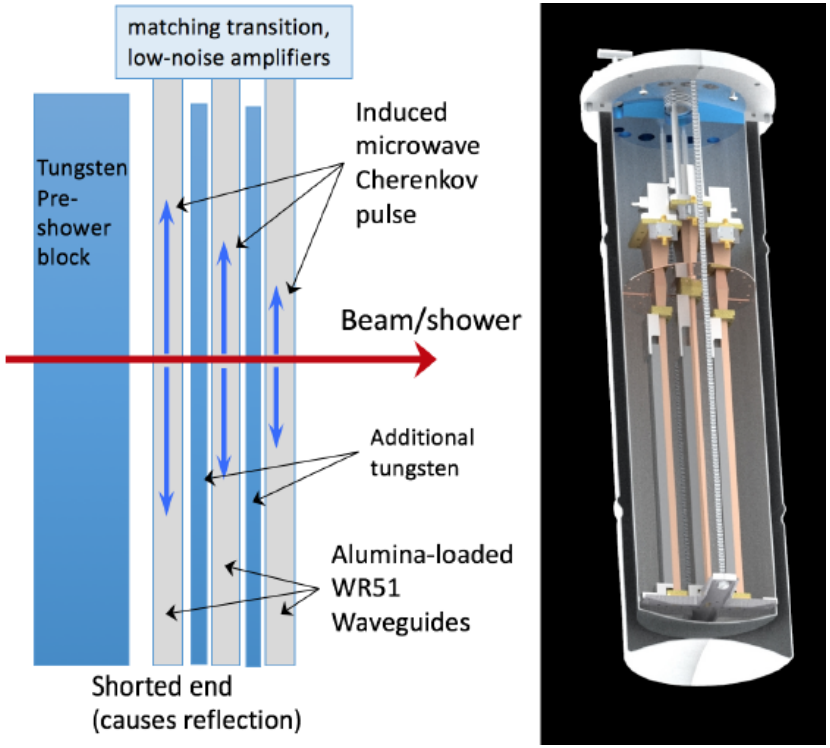
P. Orel and G. Varner

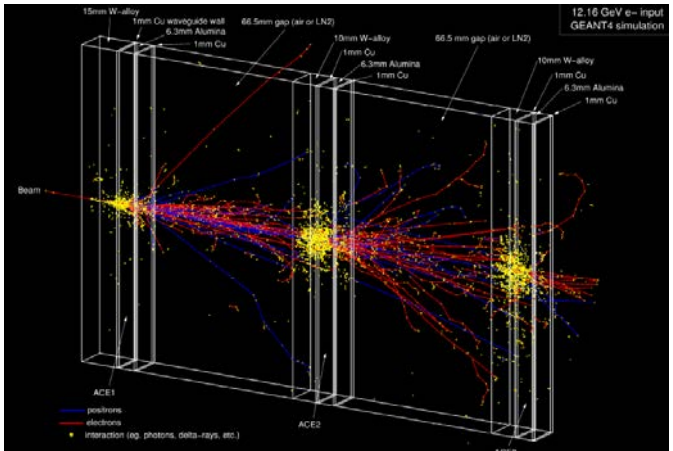
IEEE Trans. Nucl. Sci. **64 (2017) 1950-1962**.



A very different kind of DIRC detector

Askaryan Calorimeter Exp (ACE)



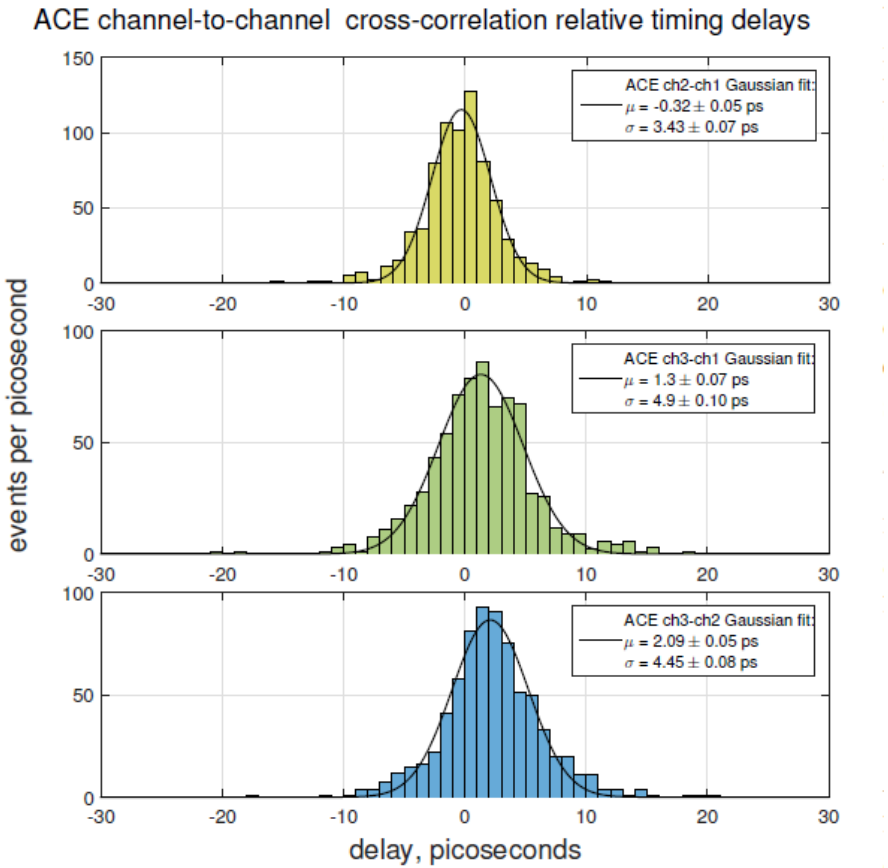


Radio (mm wave)

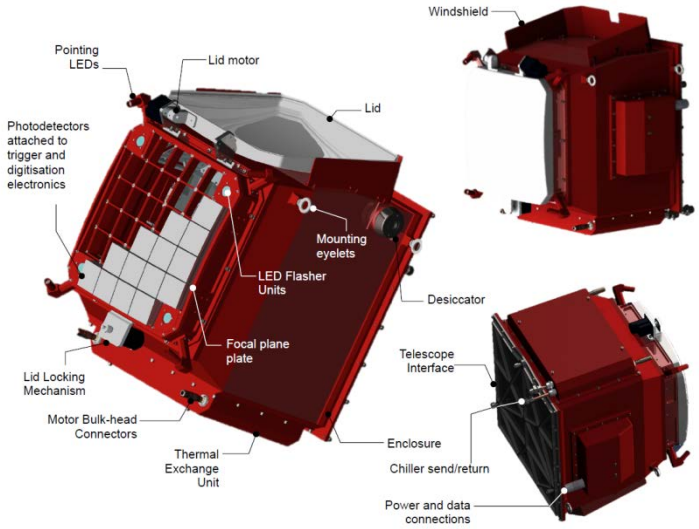
arXiv:1708:01798 (5-AUG-2017)

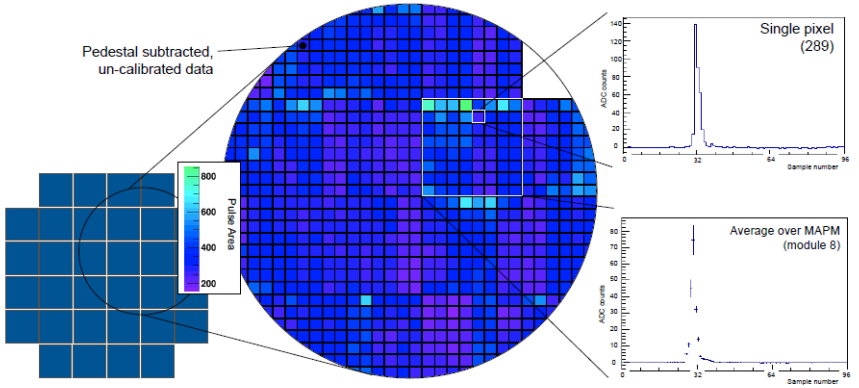
2.3ps intrinsic timing resolution

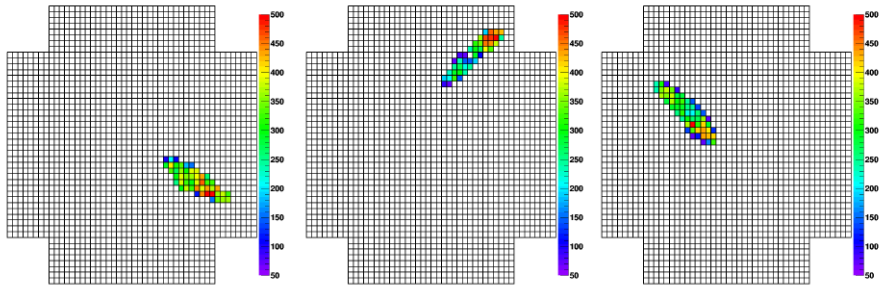
(SLAC ESTB measurement)

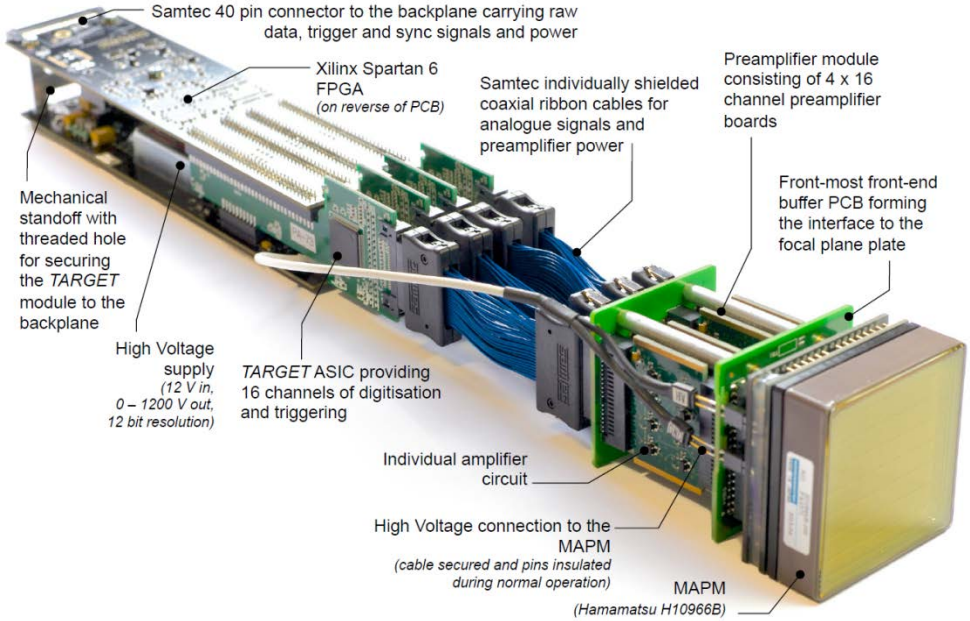


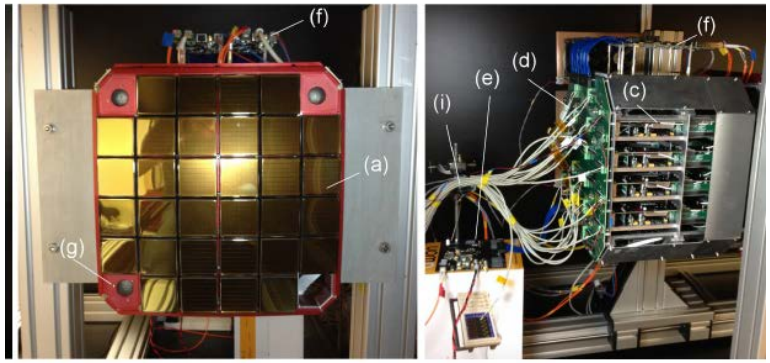
GCT Camera (CTA) – TARGET ASIC



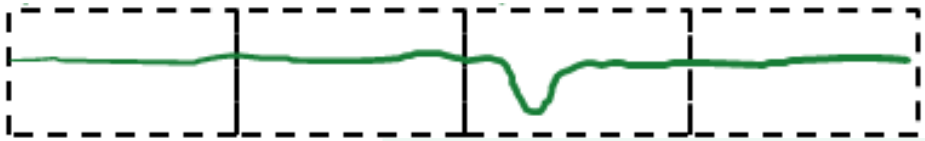


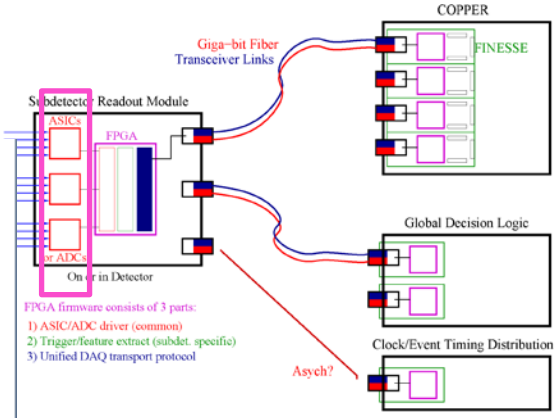






TARGET ASIC Overview





TARGET Single Channel

- Sampling: 64 (2x 32) separate transfer lanes

  Recording in one set 32, transferring other ("ping-pong")

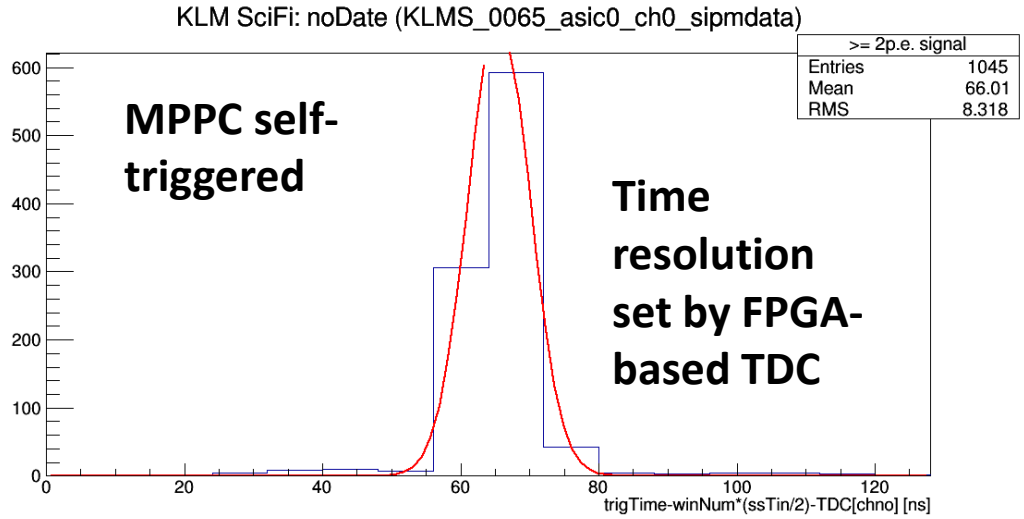
- Storage: 64 x 256 (256 = 8 * 32)

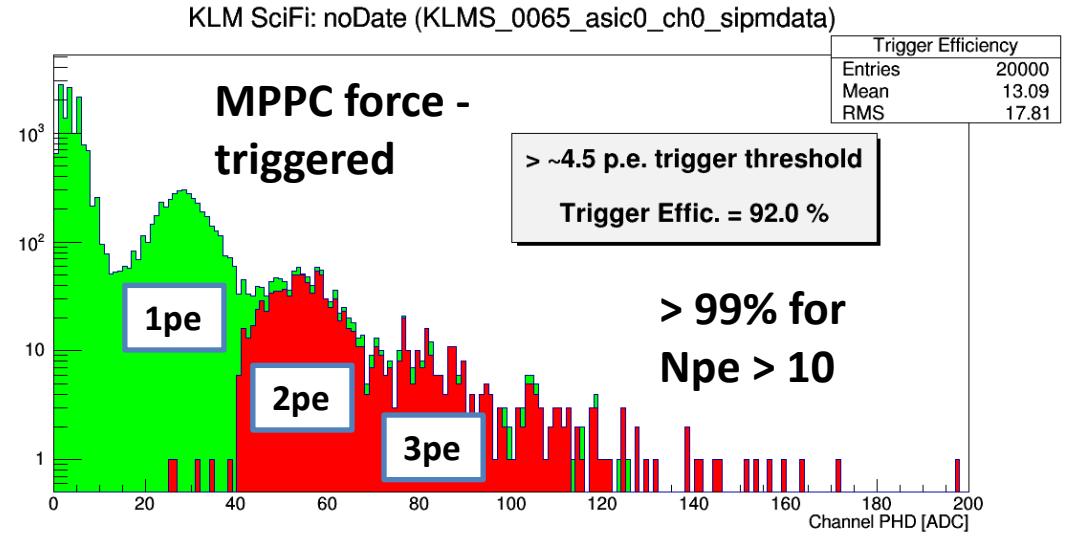
- Wilkinson (32x1): 32 conv/channel

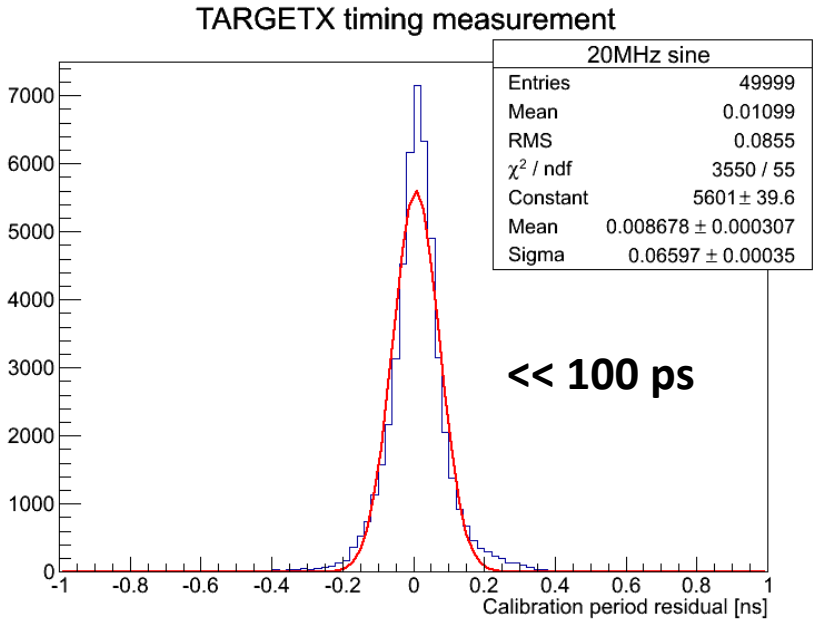
Density evolution:

- Sampling aligned to global Reference clock
- 2x more channels
- Sampling 3x slower
- Expanding next generation to 64 channels, on-chip feature extraction

Performance Reference







Sine scan data (zero crossing)

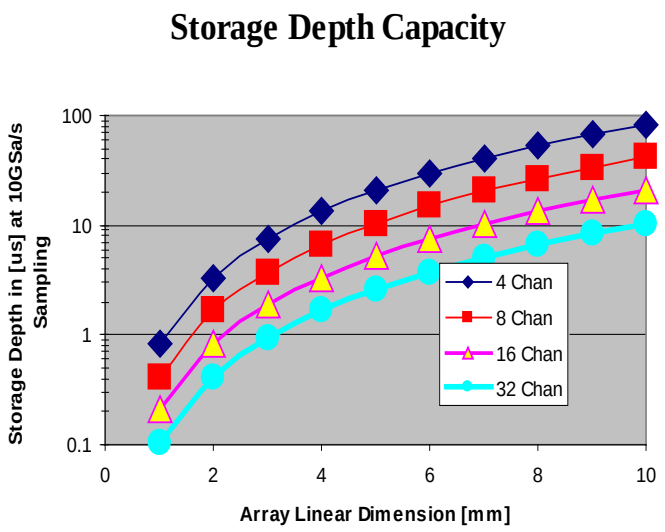
TARGET family Synopsis

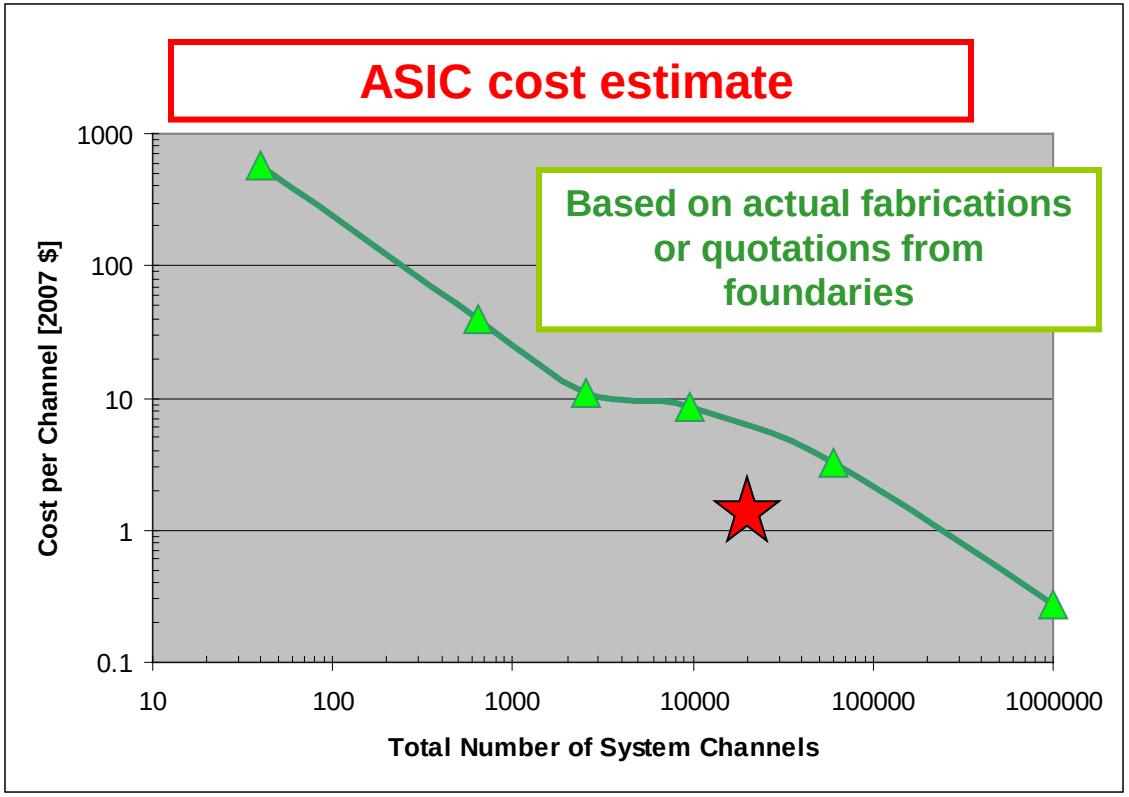
- ~21000 channels of TARGETX deployed for Belle II K-long and Muon system scintillator upgrade
- Each CTA camera 2048 channels
- 256k storage cells per ASIC (>300 million tested)
- 16 channel density attractive for compact sensor arrays (e.g. high-density DIRC …)
- **64 channel version** (SiREAD) in design
- Engineering run quantities: **$1.40/channel** (ADC and trigger on-chip)
- While not for precision timing, **< 100ps**

Looking back on >10 year development

- ASIC costing well understood, very competitive!

NIM A591 (2008) 534-345.





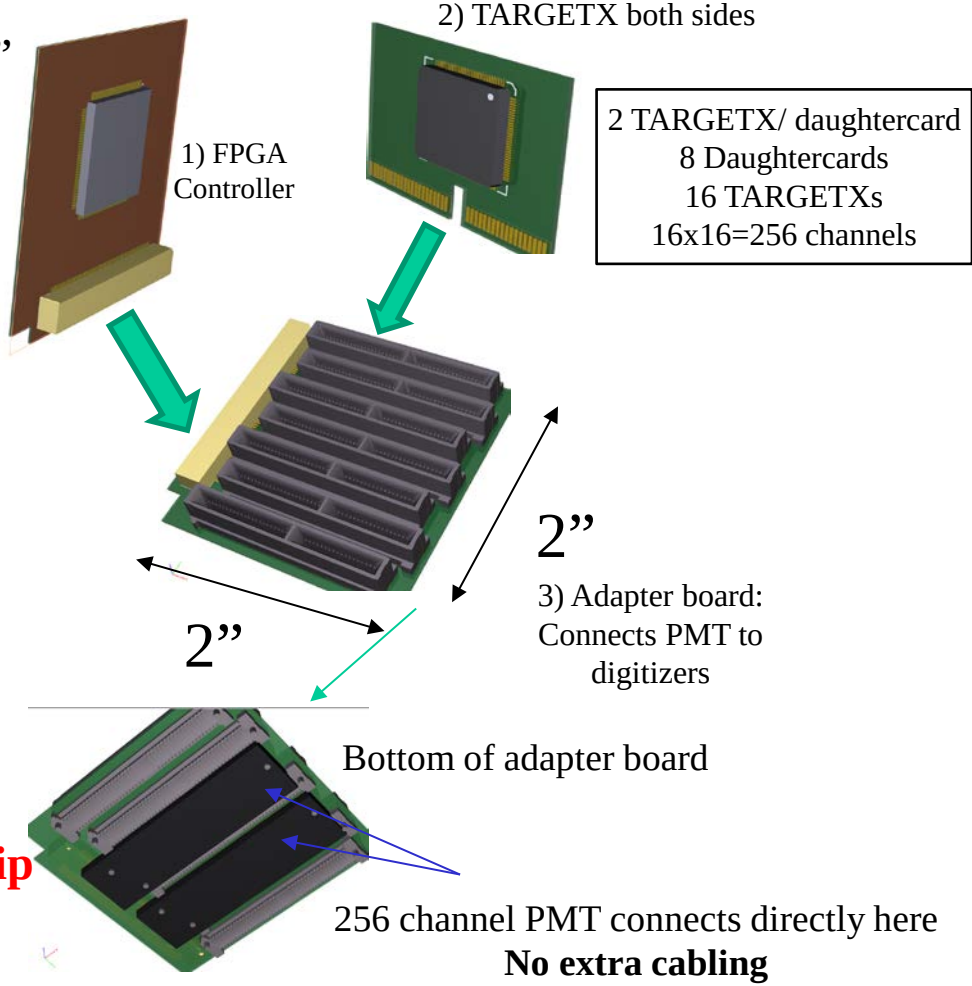
One example: modular RICH readout

Challenge:

- Readout of compact H13700 MCP-PMT
- Compact and dense: 256 channels in 2”x2”
- Timing resolution: ~100ps
- Long buffer
- Abutted Photosensors
- Likely convert to SiPM array later
- Minimize analog cabling

Solution:

- 1st gen prototype based on existing TARGETX ASIC:
  - 1GSa/s full waveform sampling
  - 16 us trigger buffer
  - 16 channels
  - Self triggering capability
  - Low cost 250nm CMOS
  - **Upgrade to 64-channel SiREAD chip**



Nalu Scientific
Data Acquisition Systems

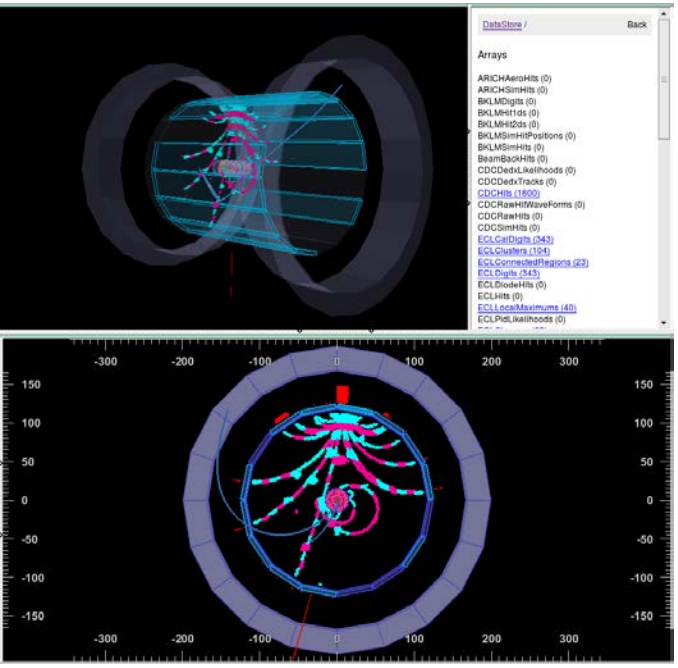
University of Hawai‘i Mānoa

Summary

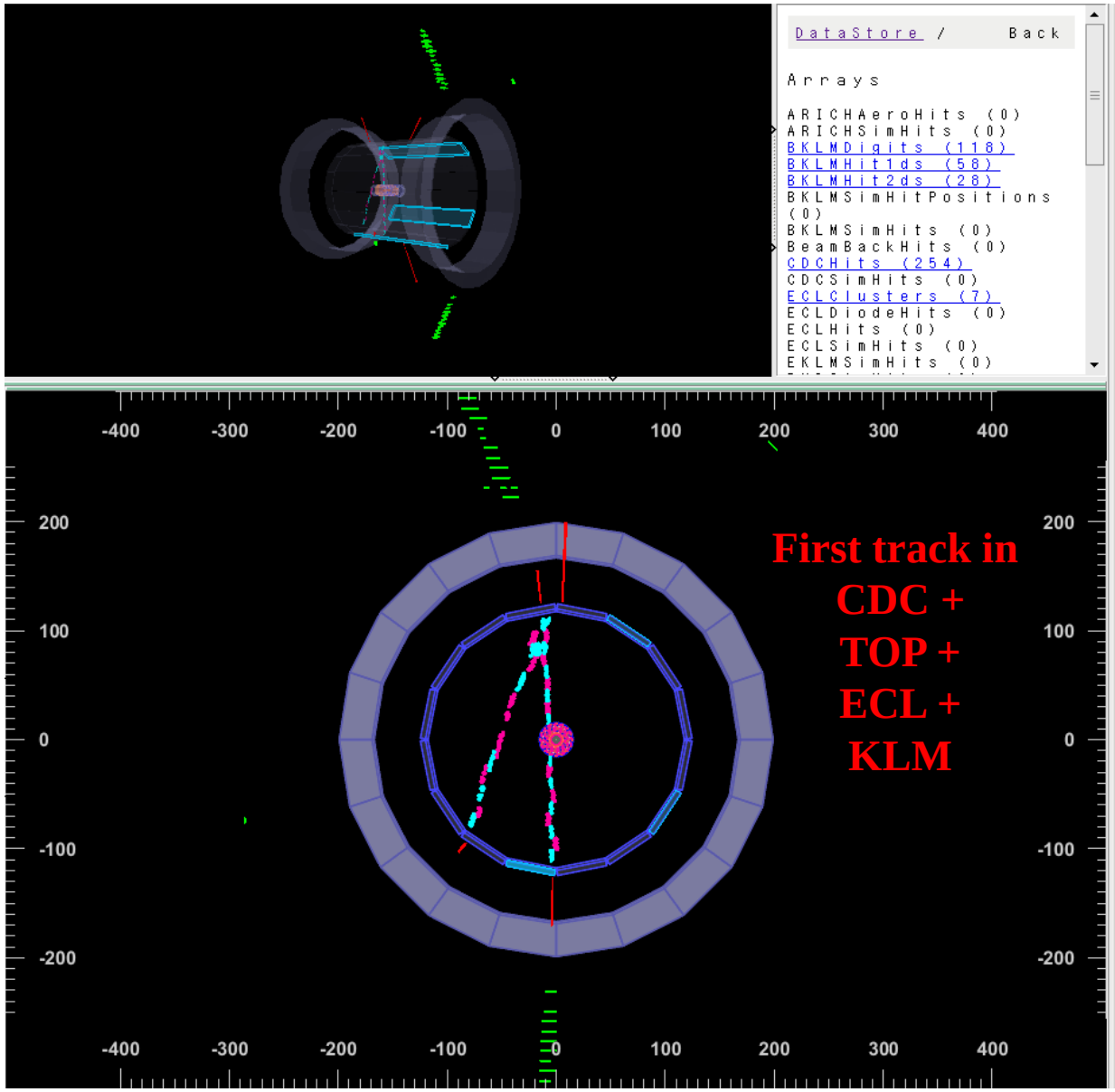
Waveform-sampling readout, directly married to photodetectors is an almost ideal DIRC readout

- **Cost:**
  - **Reduce cabling, power requirements**
  - **Underlying technology inexpensive, powerful**
- **Performance:**
  - **Space-time photon resolution PD determined**
  - **High rate, pile-up robustness**
- **Maturity:**
  - **Complex firmware biggest headache**
  - **In-ASIC functionality, commercial support**

Backup



First showering Event: CDC + TOP + ECL



First track in CDC + TOP + ECL + KLM

Calibration Procure

- What we have to calibrate for timing;

Alignment

$$\chi^2 \equiv -2\sum_{i}^{n} \log \mathcal{L}_{\mu}^{(i)}(\hat{p}) = \min,$$
$$\hat{p} \equiv (\Delta x, \Delta y, \Delta z, \alpha, \beta, \gamma, t_0)$$

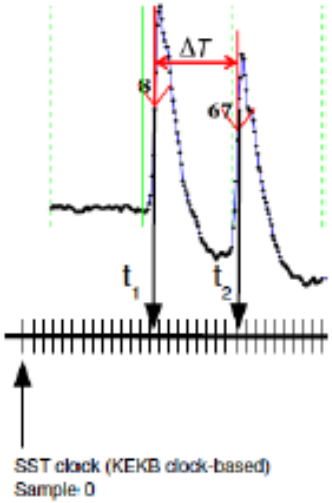
$$T_{photon} = t_{digit} + T^0_{channel} + T^0_{module}$$

Time base calibration (TBC)
Calibration of the bin size of the digitizer

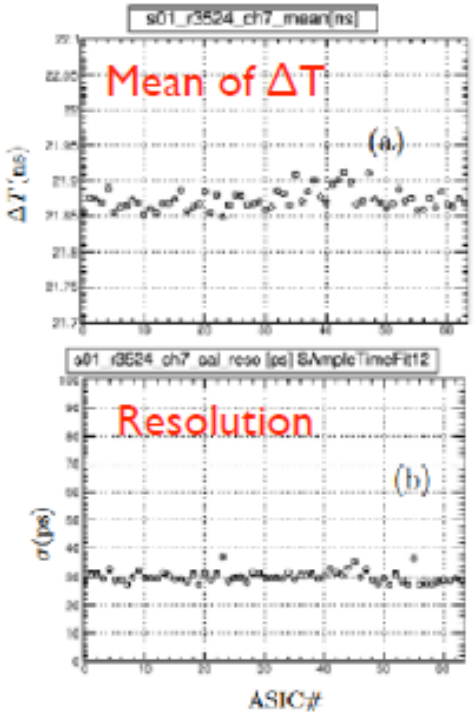
Local T0
Synchronization of the channels within a single quartz bar

Module T0
Synchronization of the modules one with the others

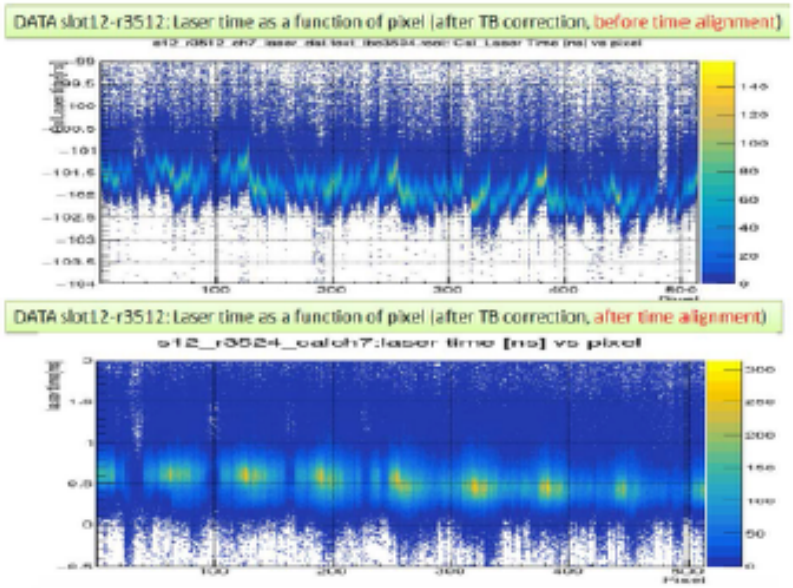
Double cal pulse



Laser calibration system



Local T0 alignment



NOTE: Very Different Time Scales!

Timebase Calibration

- Took a while to get new FW release, SW work continued

/group/belle2/users/wangxl/iTOP/TBC/DB201612b/xval/. The data of run3523 and run3524 are also processed and skimed, and finally saved at **/ghi/fs01/belle2/bdata/group/detector/TOP/Skim-wangxl/2016-12/**.

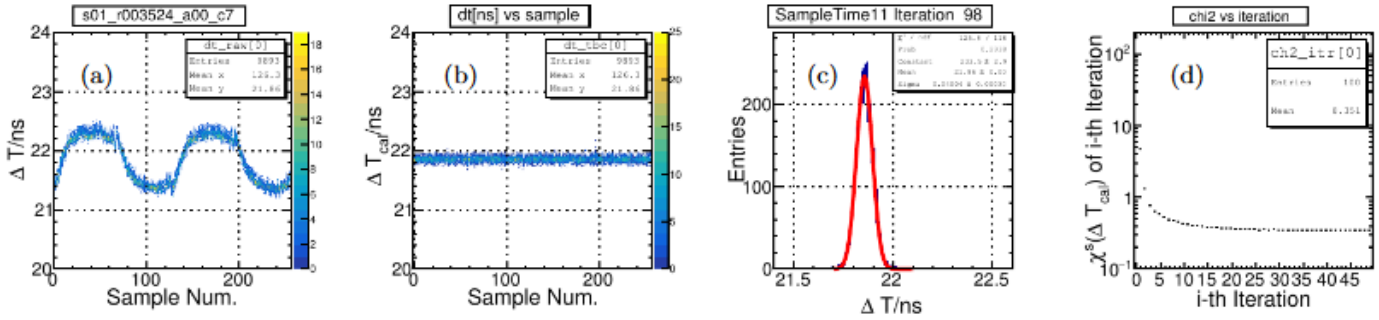


FIG. 1: Example of calculation on Slot_01 ASIC_00. (a) is the shape of time difference (ΔT) of the double pulses in channel_7 from the raw data, (b) is the dime difference after correction, (c) is the project of ΔT after correction and a fit performed to the distribution to show the mean and the resolution of ΔT, (d) shows how the χ^2 values change in the iterations of calculation.

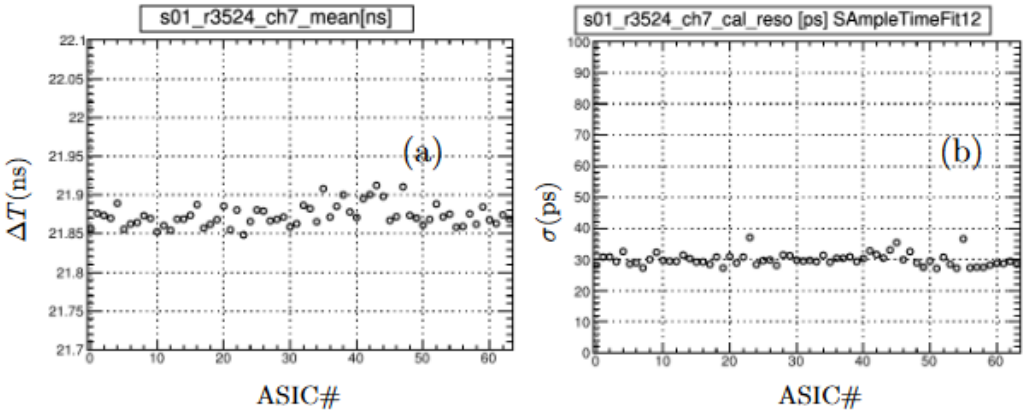


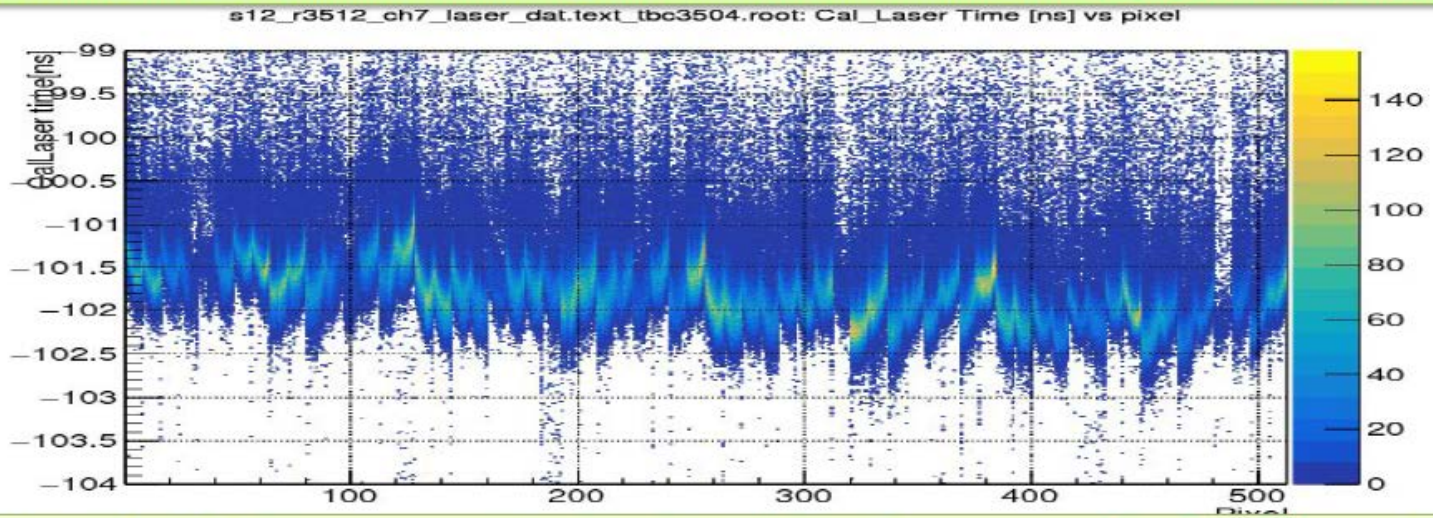
FIG. 2: Summary of calculation results of the 64 ASICs of Slot_01. Plot (a) is means of the time difference of double pulses, and (b) is the time resolution.

Channel-by-channel Timing alignment

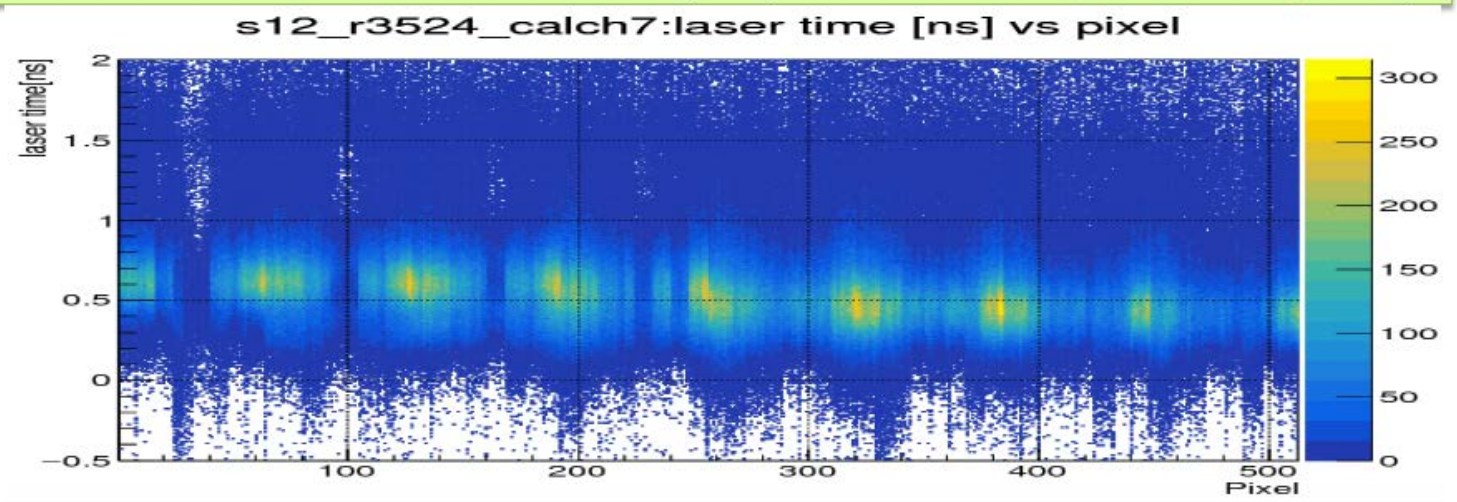
- Global timing alignment – laser studies

NOTE: Different Time Scales!

DATA slot12-r3512: Laser time as a function of pixel (after TB correction, before time alignment)

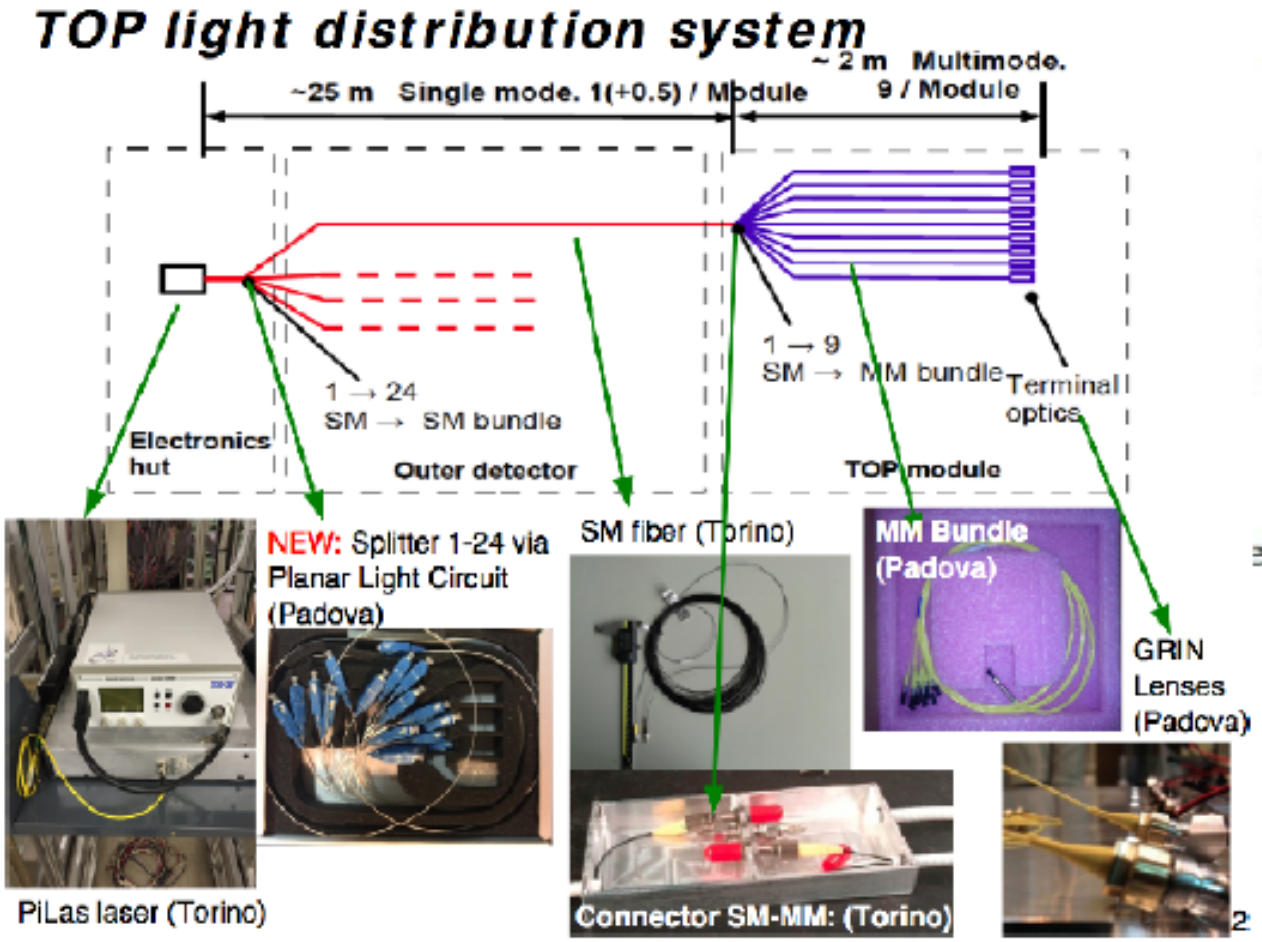


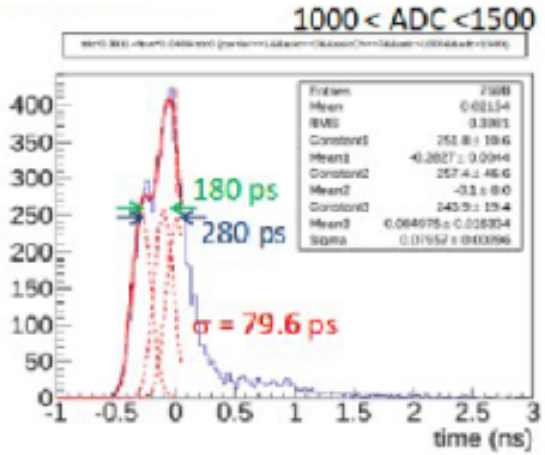
DATA slot12-r3512: Laser time as a function of pixel (after TB correction, after time alignment)



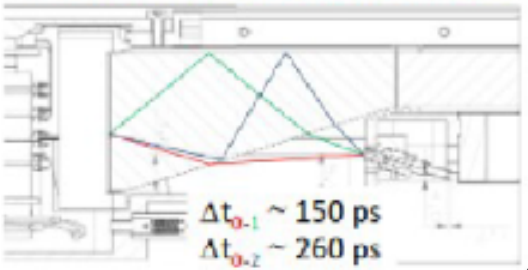
Laser timing calibration/alignment

- To synchronize the channels within a single module, we flash them with a pico-second laser pulse through optical fibers.
- The system has been developed by Italian group (Padova/Torino)

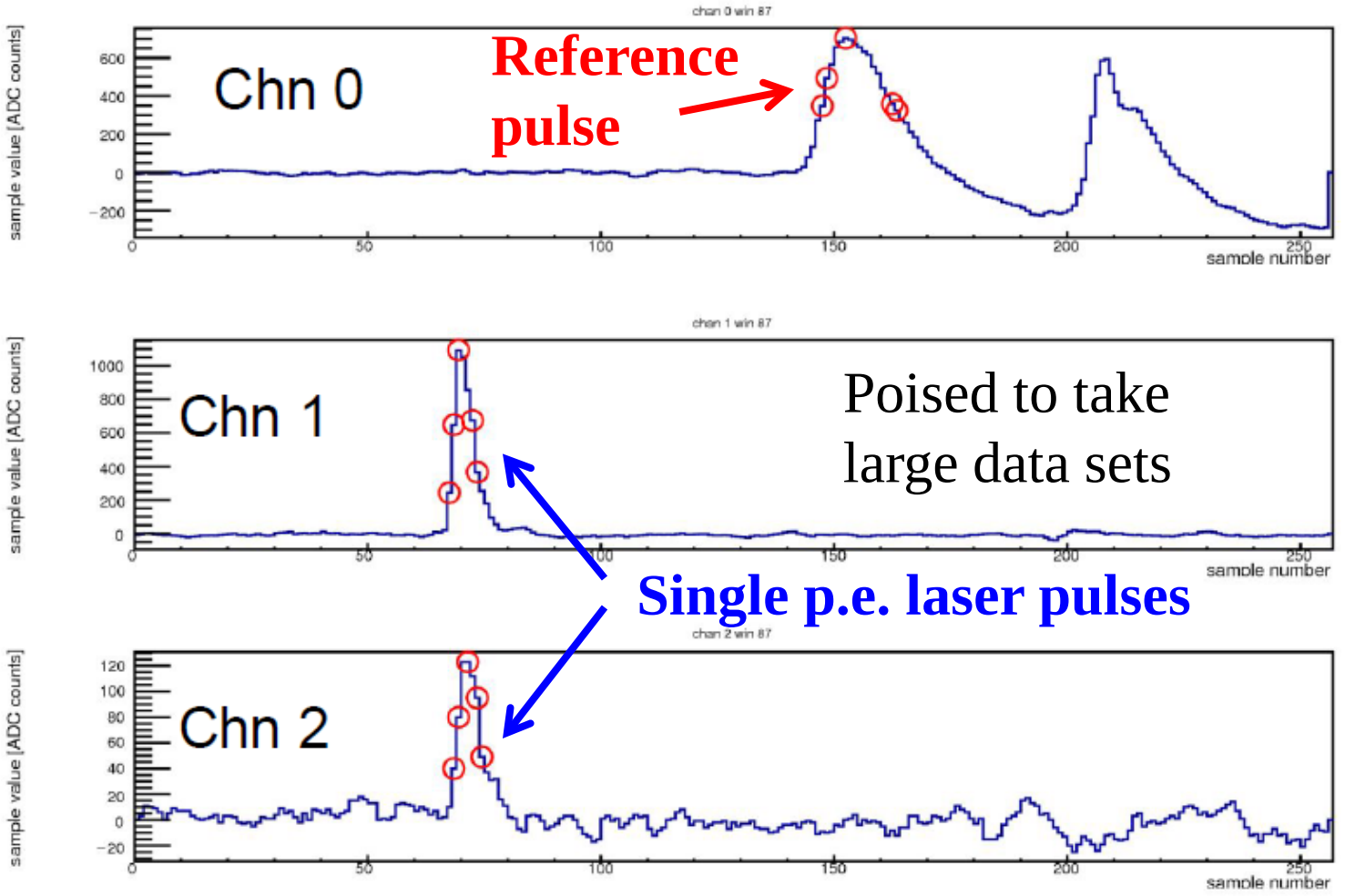




Probably three peaks by direct photons and those reflected once and twice



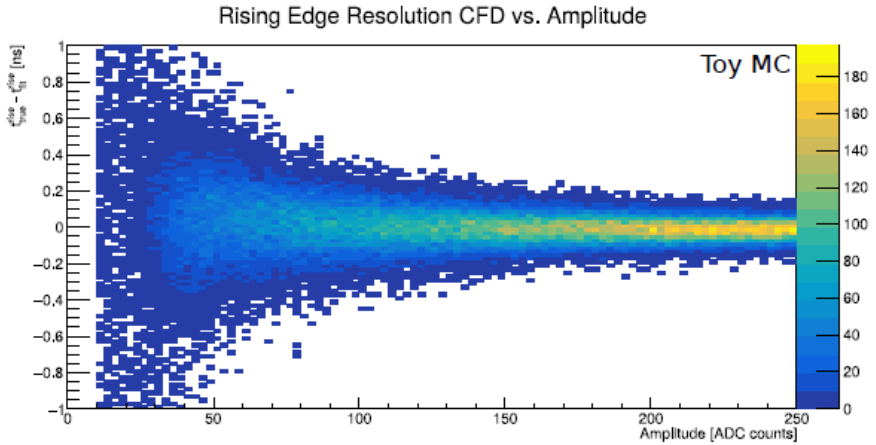
Region Of Interest & Feature Extraction



Standard CFD algorithm works well, though performance degrades at low PMT (mandated to mitigate aging effects)

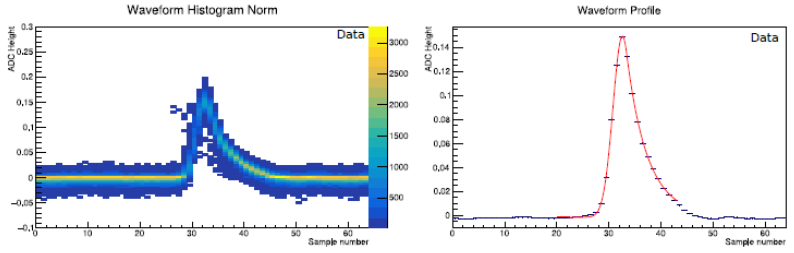
Low PMT Gain Operation

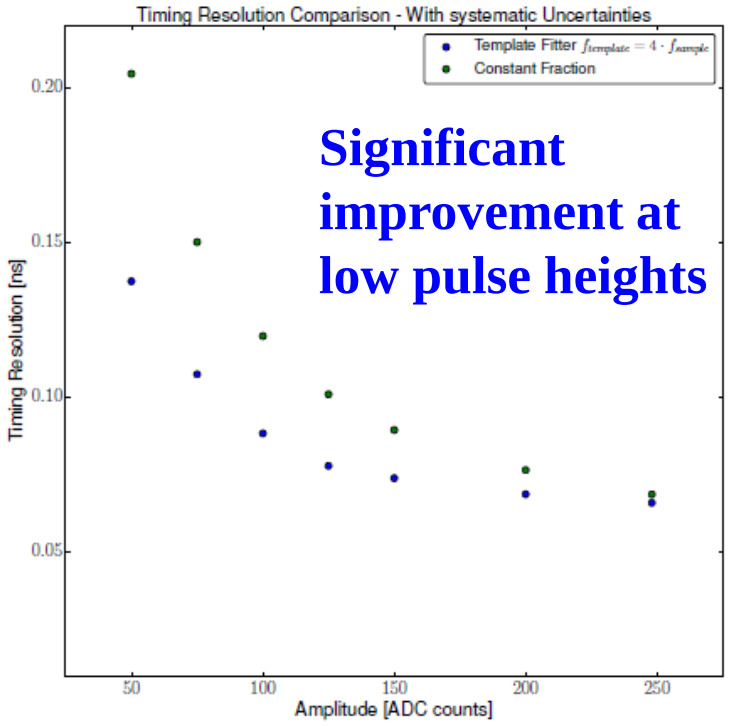
- current feature extraction uses constant fraction discrimination to extract signal timing
- resolution deteriorates at small signal amplitudes



- use template fitter to improve resolution at small amplitudes/high noise

- using laser data from Hawaii test setup
- TProfile to get waveform template
- fit with central Gaussian and exponential tail



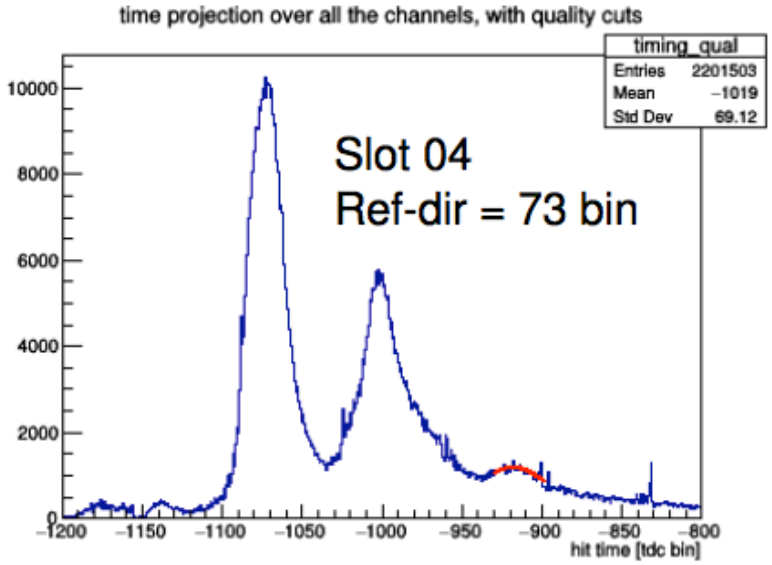


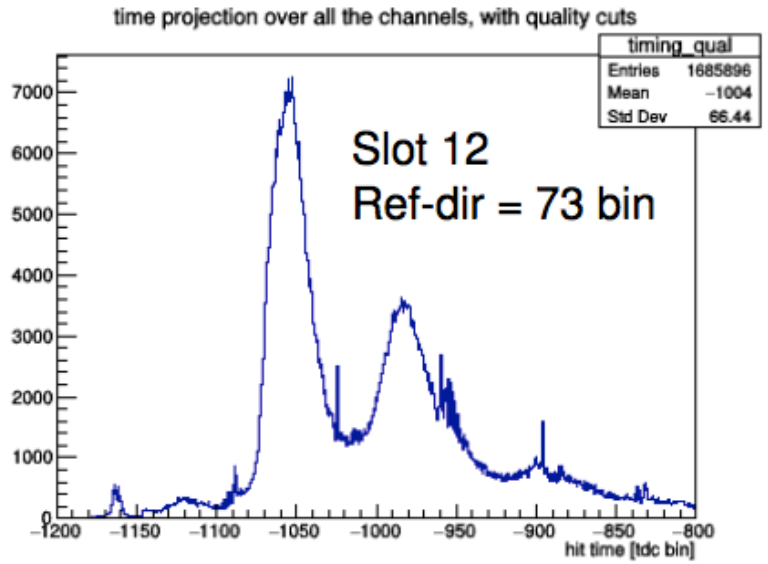
Significant improvement at low pulse heights

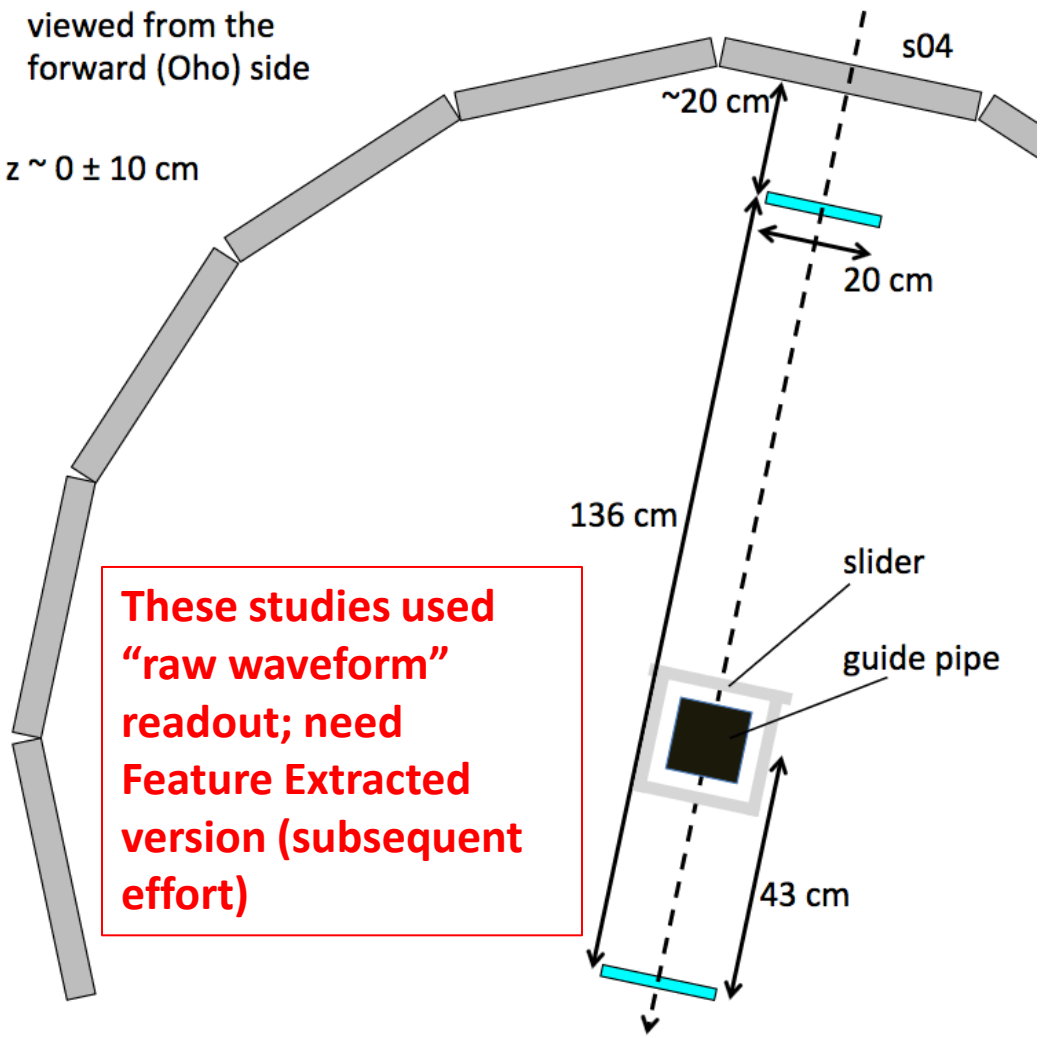
Necessary to maximize MCP lifetime

Studying how best to implement (Zynq: PS is too slow(?), PL option)

After installation – comparison plot



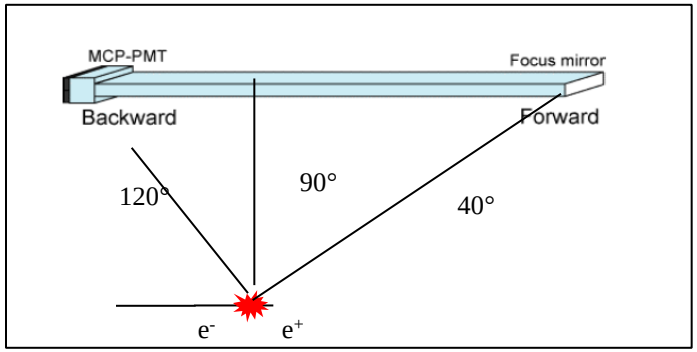




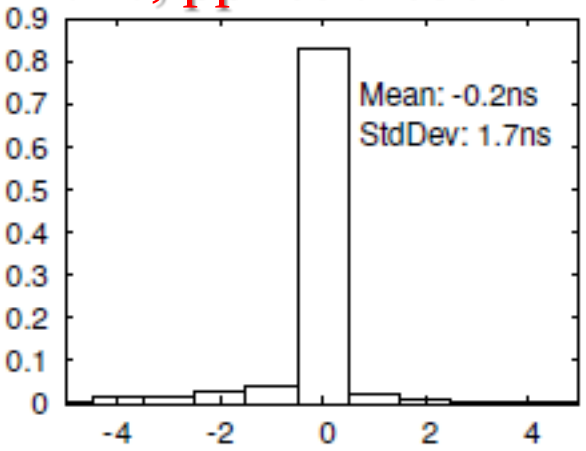
These studies used "raw waveform" readout; need Feature Extracted version (subsequent effort)

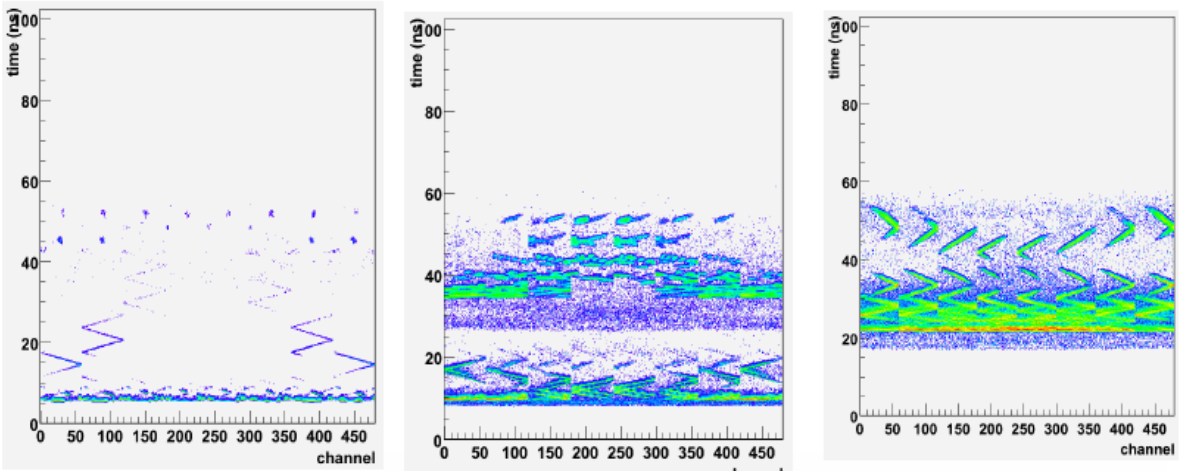
iTOP Trigger Requirements

- Few ns time resolution triggering



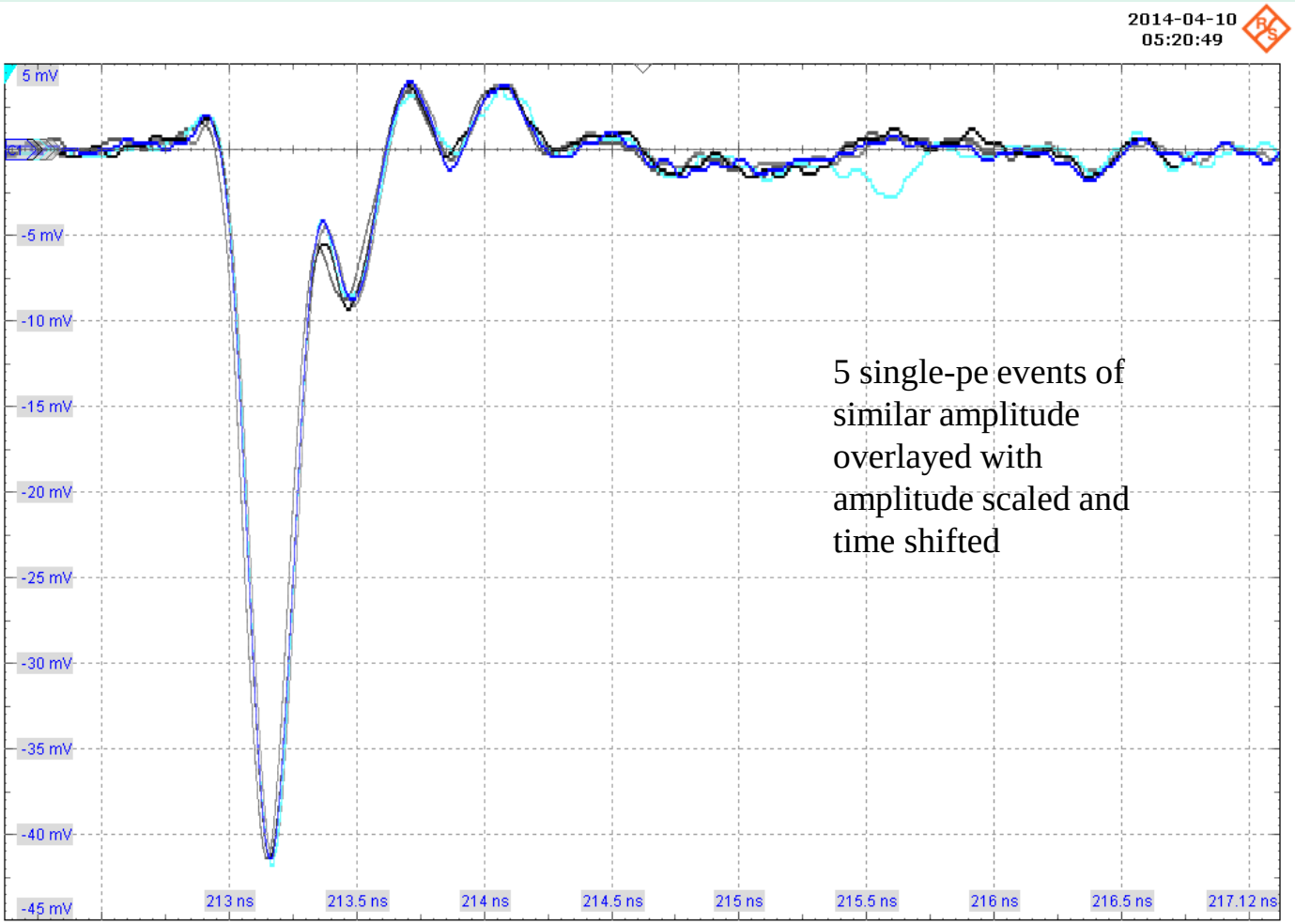
X. Gao *et al.*, IEEE (NSS/MIC) proceedings, 2010, pp 630-635.





Single-track performance

PMT signal transmission through front board and pogo pins to (mock) carrier board



scope 4GHz BW 20 GS/s 500 ps/div 5 mV/div ext. att. 0.83
Risetime of these pulses ~130 ps