

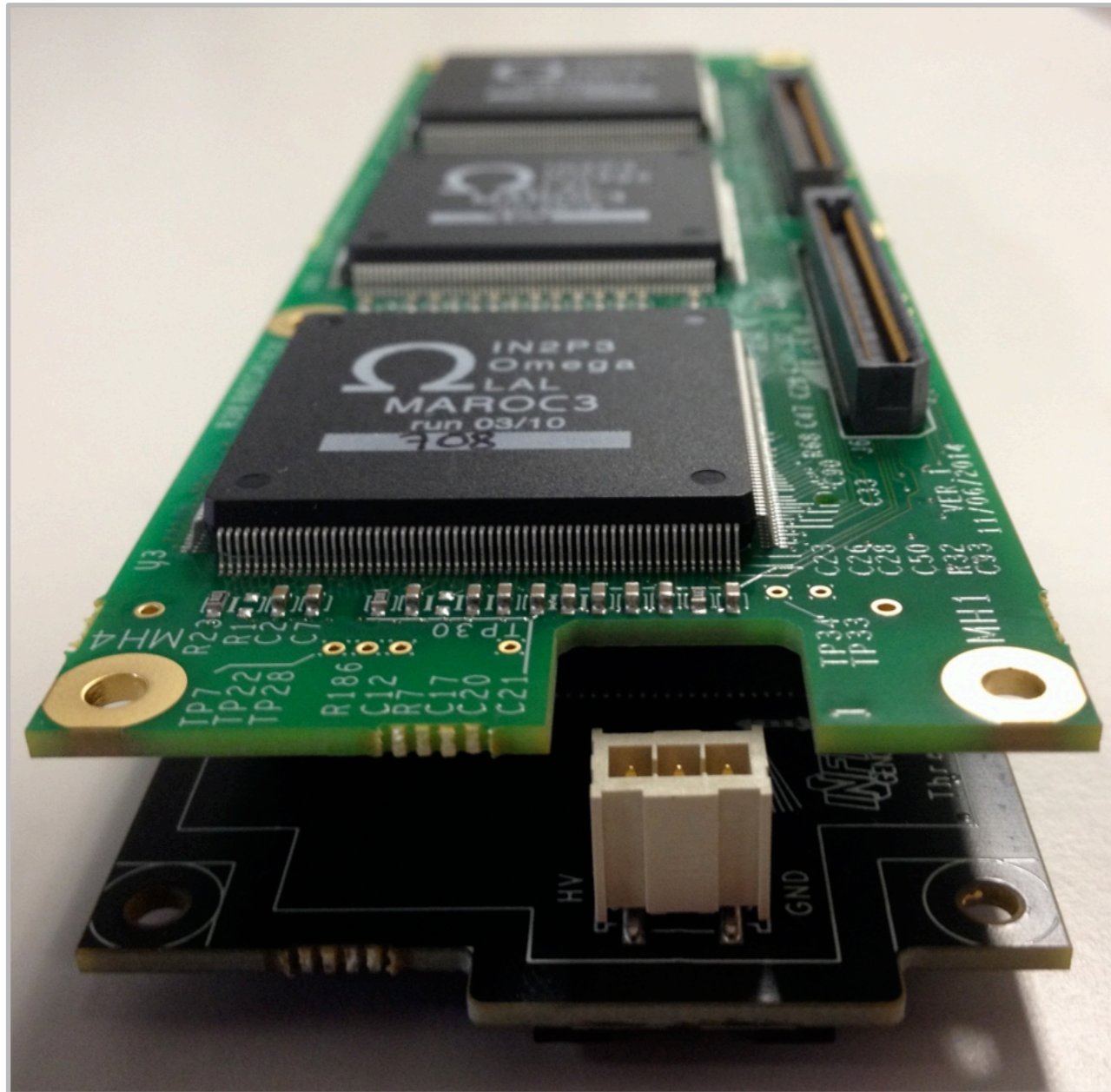
CLAS12 RICH front end electronics

Matteo Turisini - INFN - Ferrara - Italy
on behalf of CLAS12 RICH electronics group

November 11-13, 2015 - Castle Rauschholzhauser, Justus-Liebig-Universität Giessen



Overview

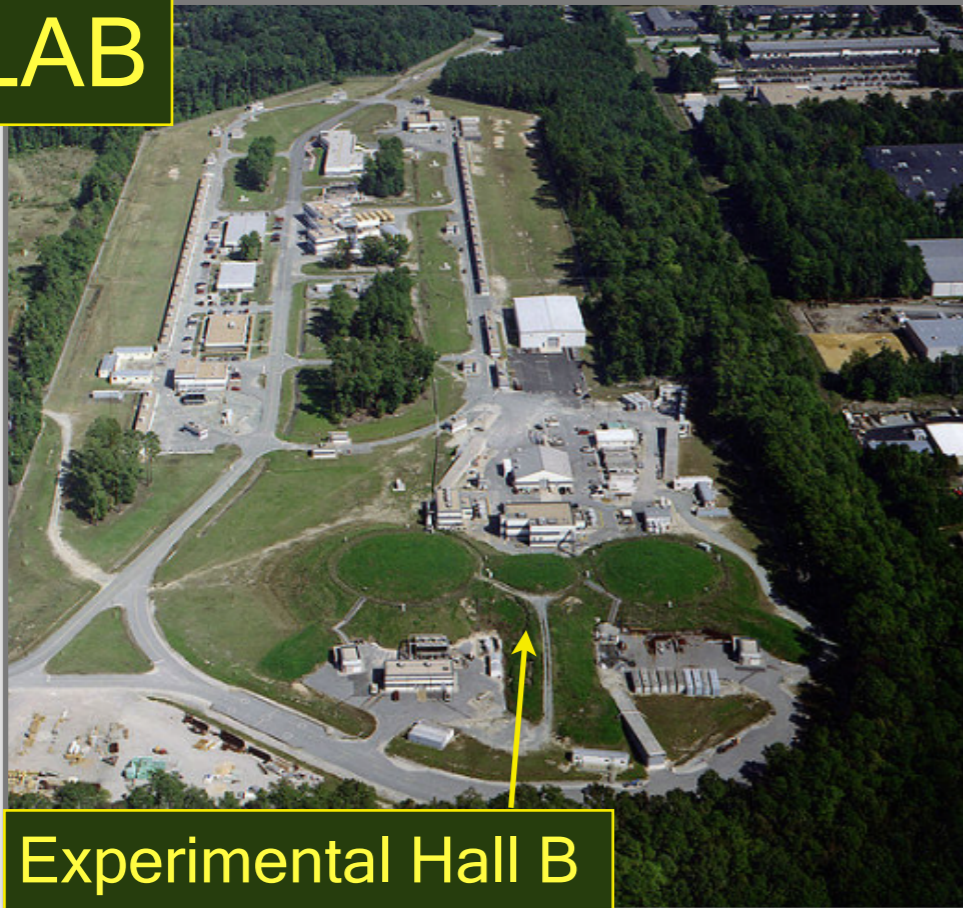


CLAS12 RICH project
 Electronics Requirements
 Hardware design
 Performance

CLAS12

at Thomas Jefferson National Laboratory, Newport News, Virginia, USA

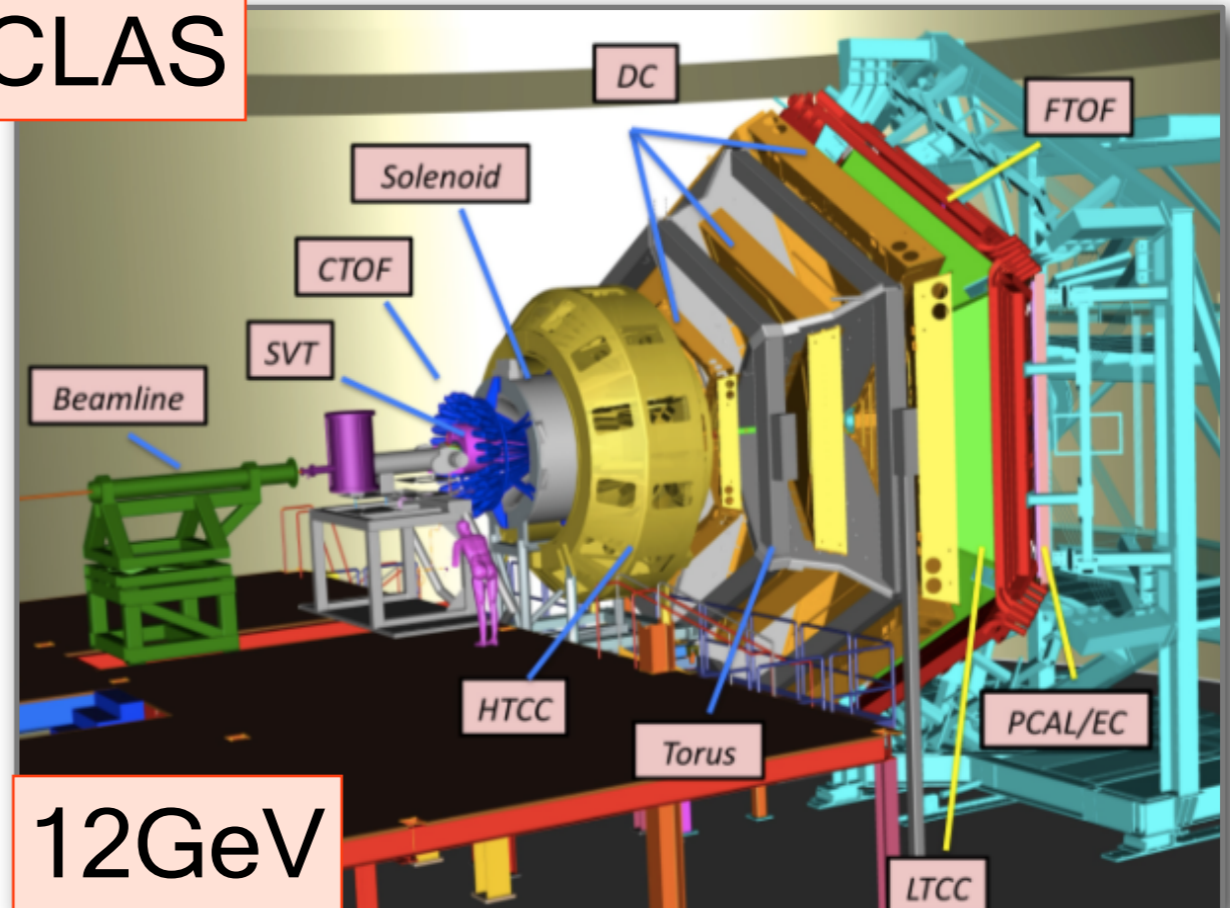
JLAB



Experimental Hall B

Continuos Electron Beam Accelerator Facility (CEBAF)

CLAS



12GeV

CEBAF Large Acceptance Spectrometer (CLAS)

RICH will be installed in the CLAS12 spectrometer in the Hall B of JLAB

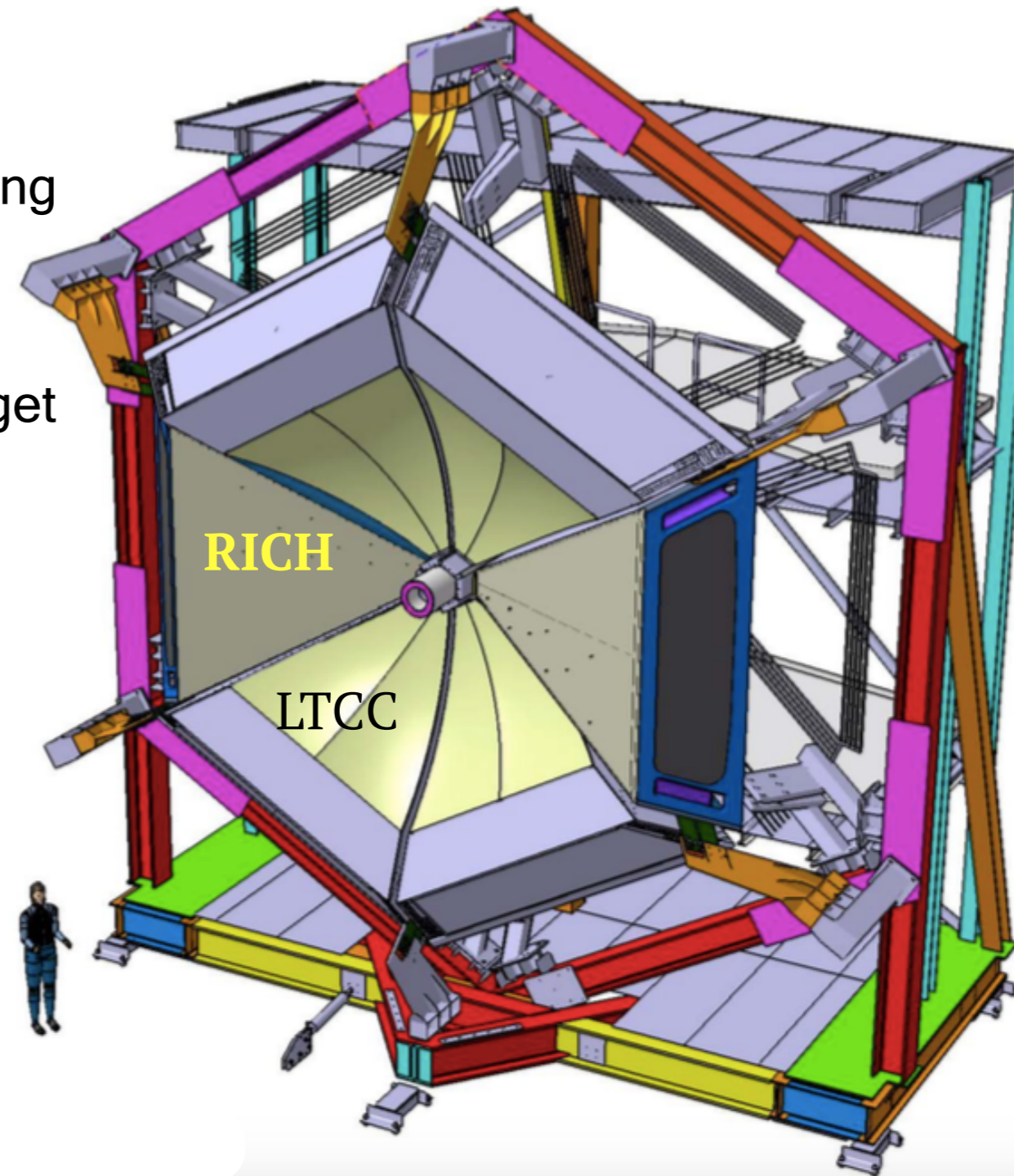
RICH Project

Replace conventional Cherenkov (LTCC) to achieve excellent K/Pi separation

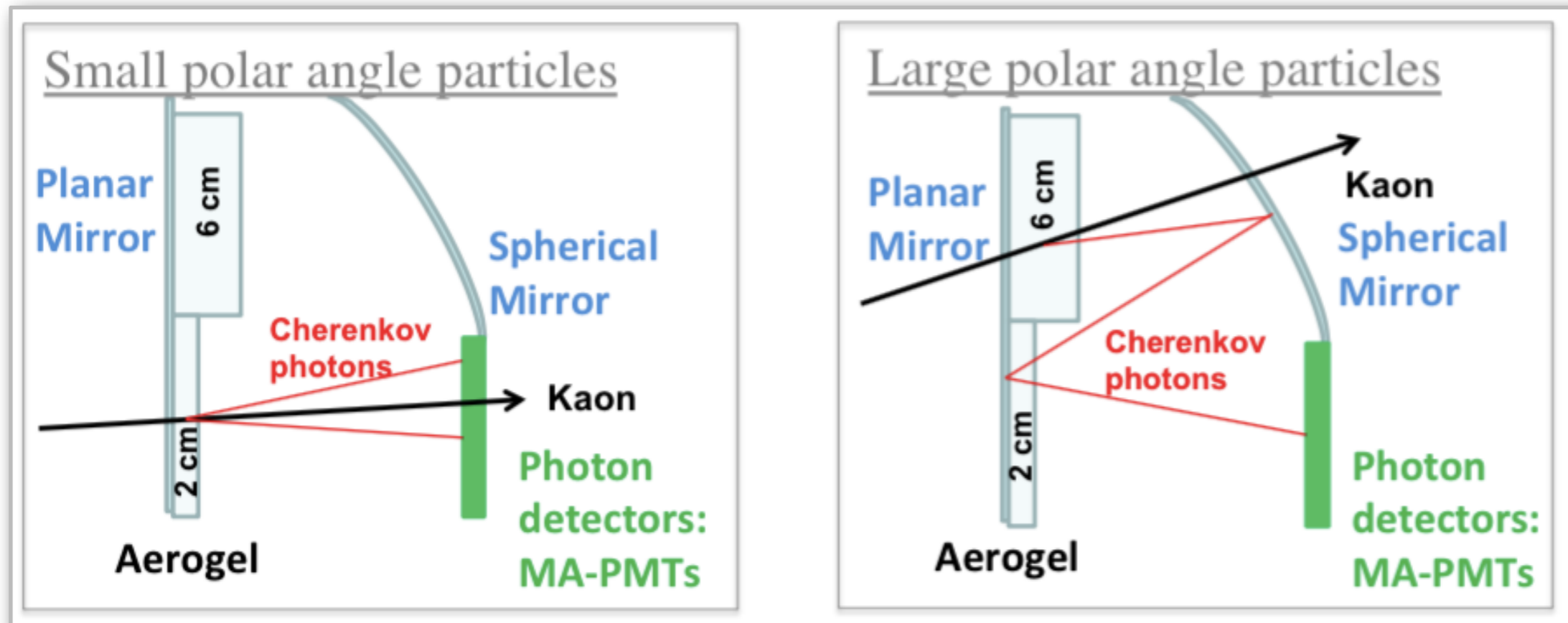
- First sector:
ready for the beginning of CLAS12 data taking
- Second sector:
Symmetric setup for transverse polarized target

International collaboration

(Italy, USA, Korea, Germany, Chile, UK)

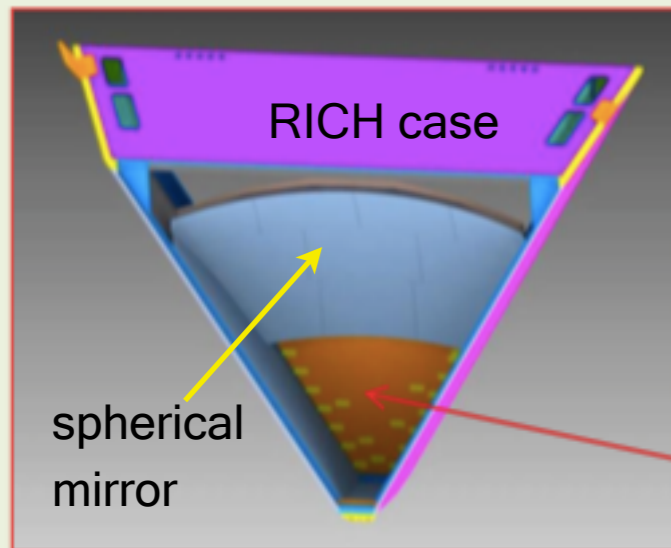


RICH Design



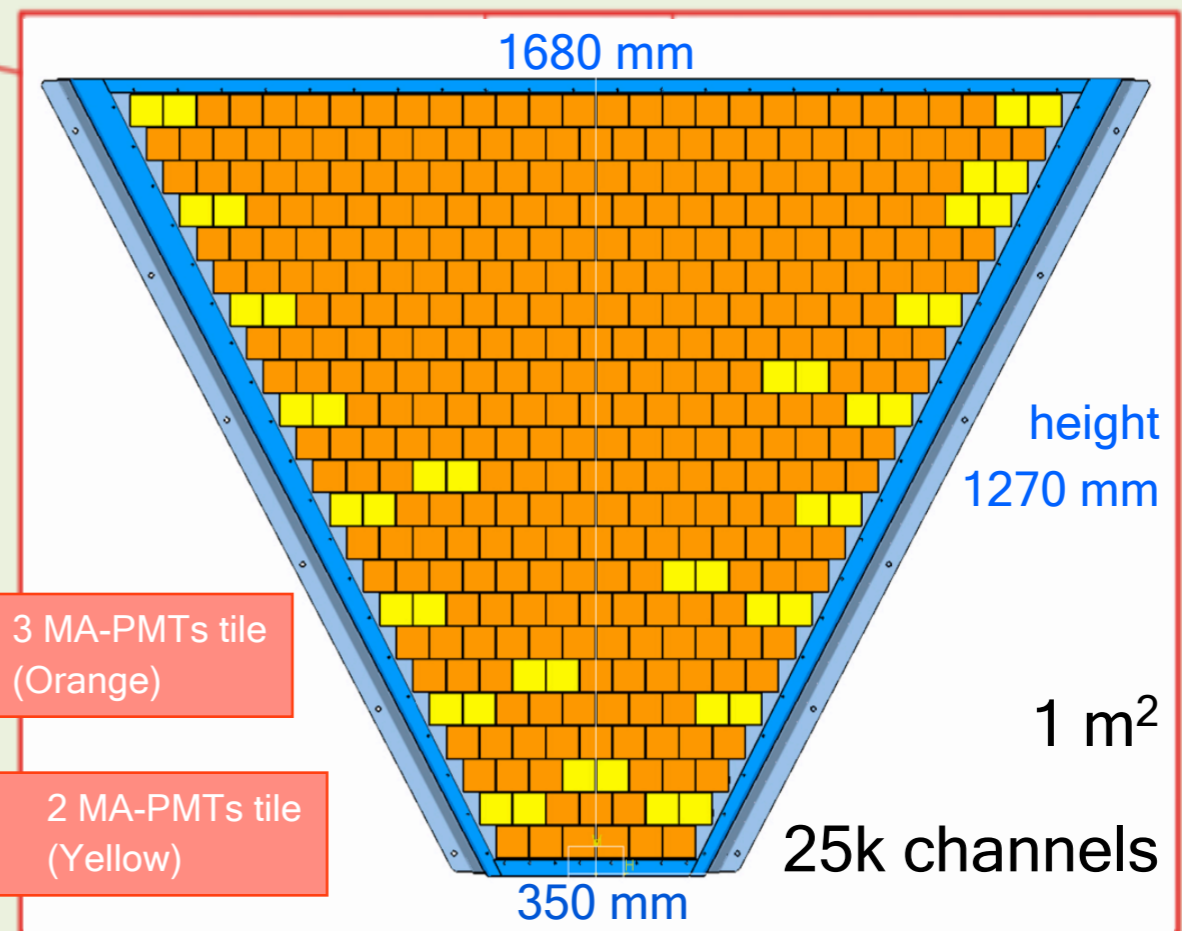
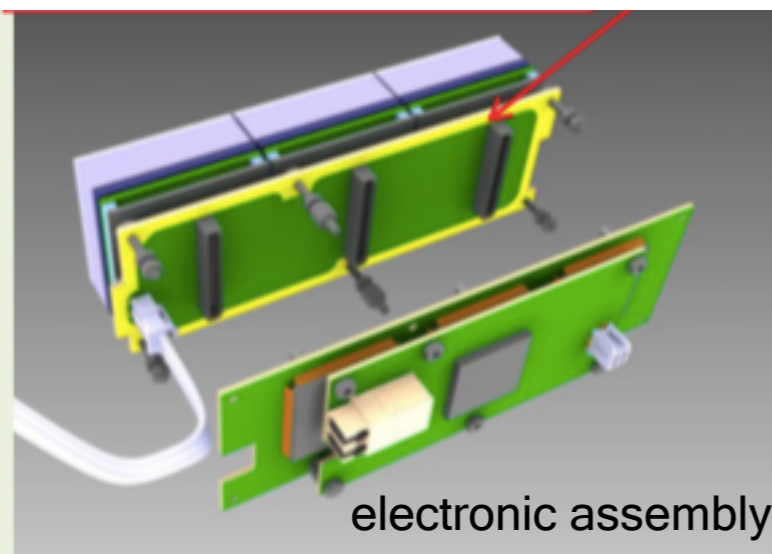
- Hybrid geometry reduces instrumented area (1 m², 25k channels, MA-PMTs)
- Detector concepts validated at CERN T9 (December 2012) [NIM A766 \(2014\) 22](#)
- Aerogel radiator to cover the momentum range 3-8 GeV (optical photons)
- Isolated N₂ volume to avoid moisture

RICH Electronics Panel



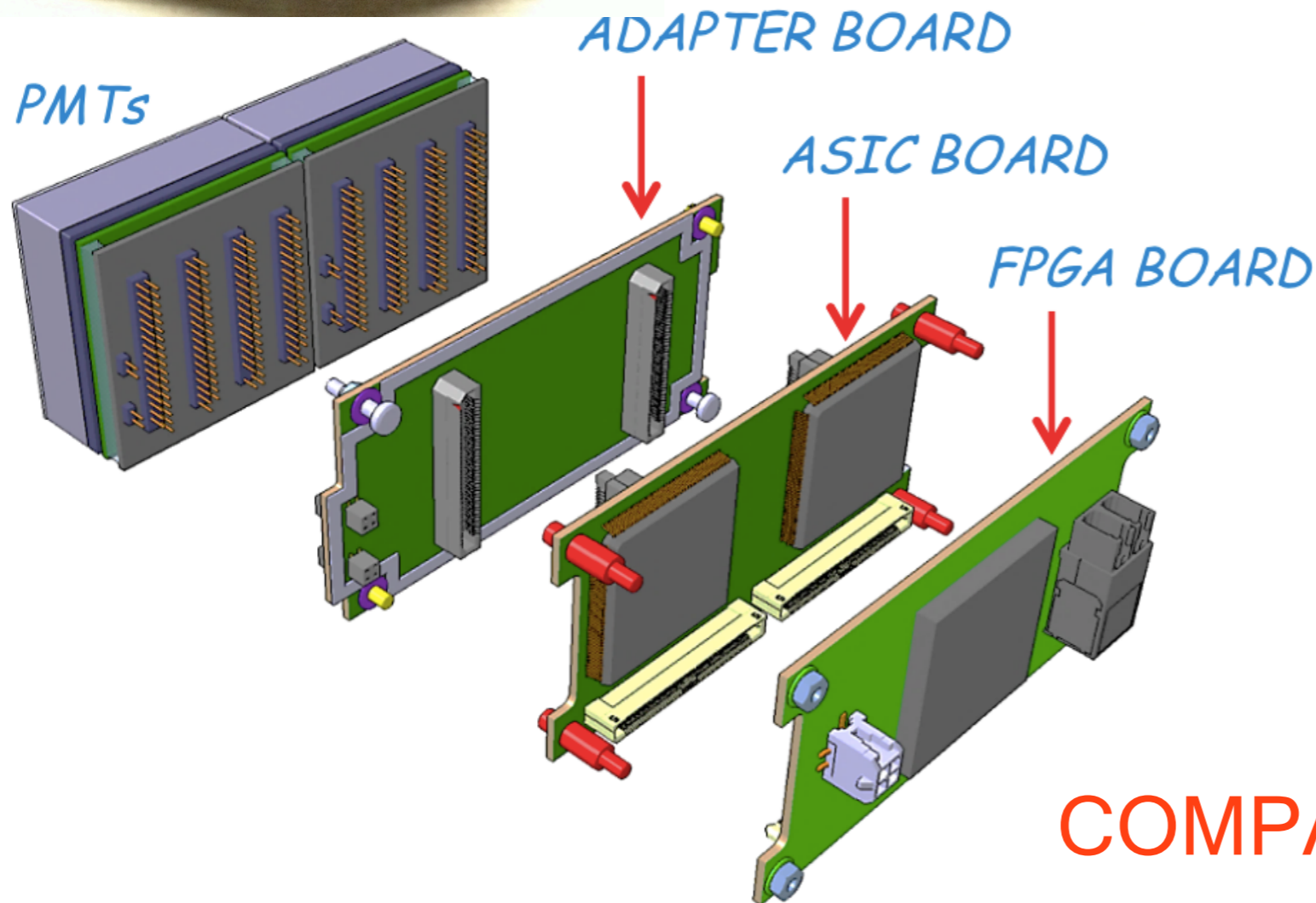
Tessellation approach: 2 or 3 MA-PMT tiles
Services out of acceptance (lateral loglines)

400 Hamamatsu MA-PMTs
H8500 and H12700



single photon sensitive surface

RICH Electronics Module



CLAS12-RICH Requirements

Single photoelectron capability

Adjustable gain 1:4

Time resolution 1 ns

Trigger rate 20kHz

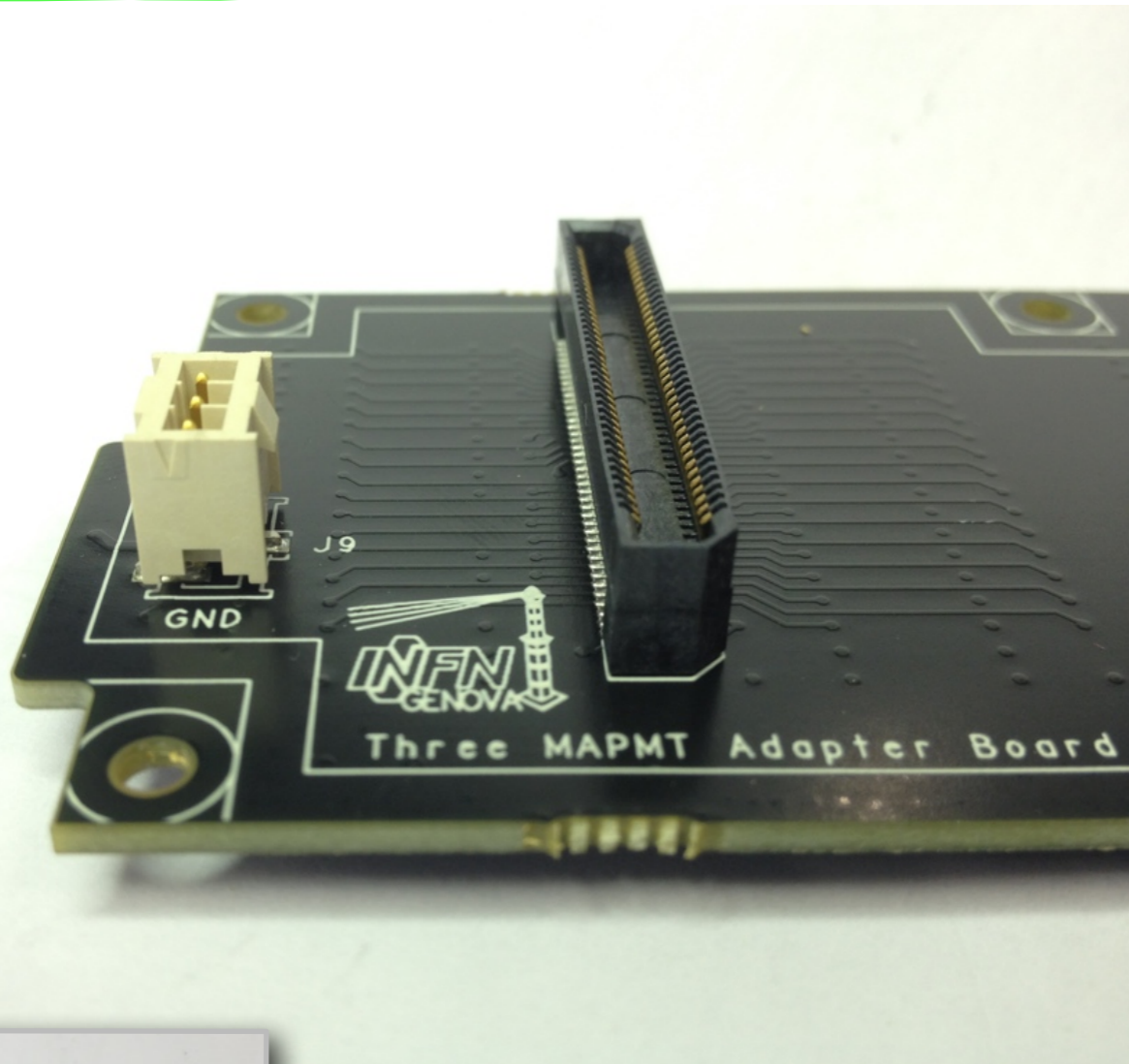
Trigger latency 8 μ s

<4 Watts/module

Radiation tolerance adequate
for CLAS12 environment

COMPACT! ON DETECTOR!!

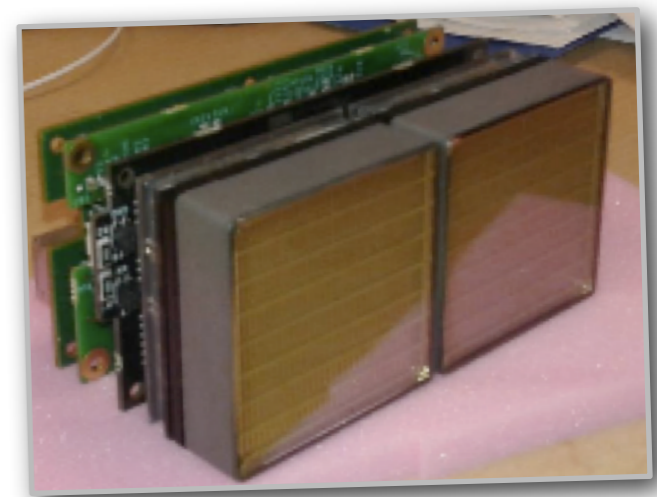
Adapter Board



- Feed through passive board:
- Distribute HV power to MA-PMTs
 - Light & gas tight
 - Low capacitance electrical connectivity with front end chip



Design to achieve 96% packaging factor
(1 mm gap between MA-PMTs)



ASIC Board

Application Specific Integrated Circuit (ASIC) board features:

Multi Anode Read Out Chip (MAROC)

- 64 inputs
- 64 outputs (binary)
- Common **THRESHOLD** (10 bits)
- Individual Preamplifier **GAIN** 0 to 4 (8 bits)
- Charge output (12bit ADC, serial)
- Highly Configurable shaping sections
- Total 829 bits for slow control

Test Pulse (12 bit DAC, 0 to 5pC)*

Voltage regulators (High Speed Transceiver Logic optimized)*



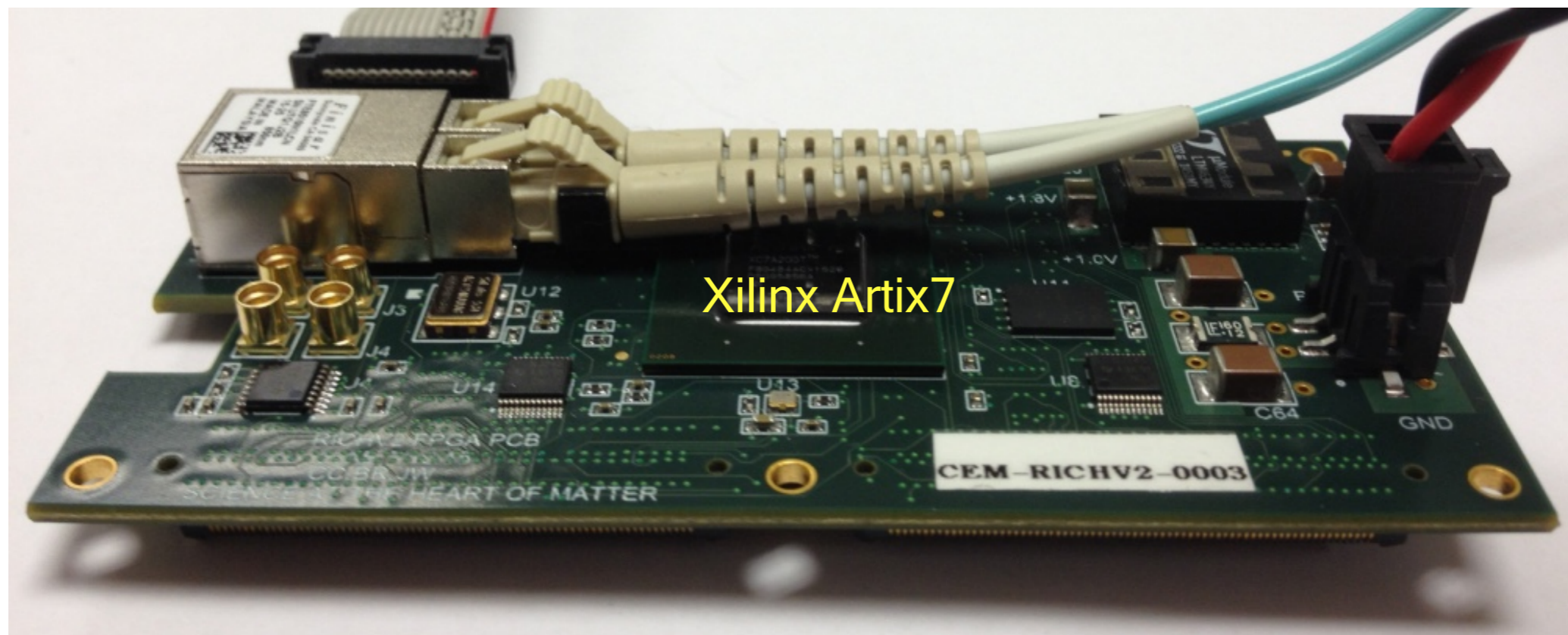
3 ASIC variant

* pre production run Dec 2015

FPGA Board

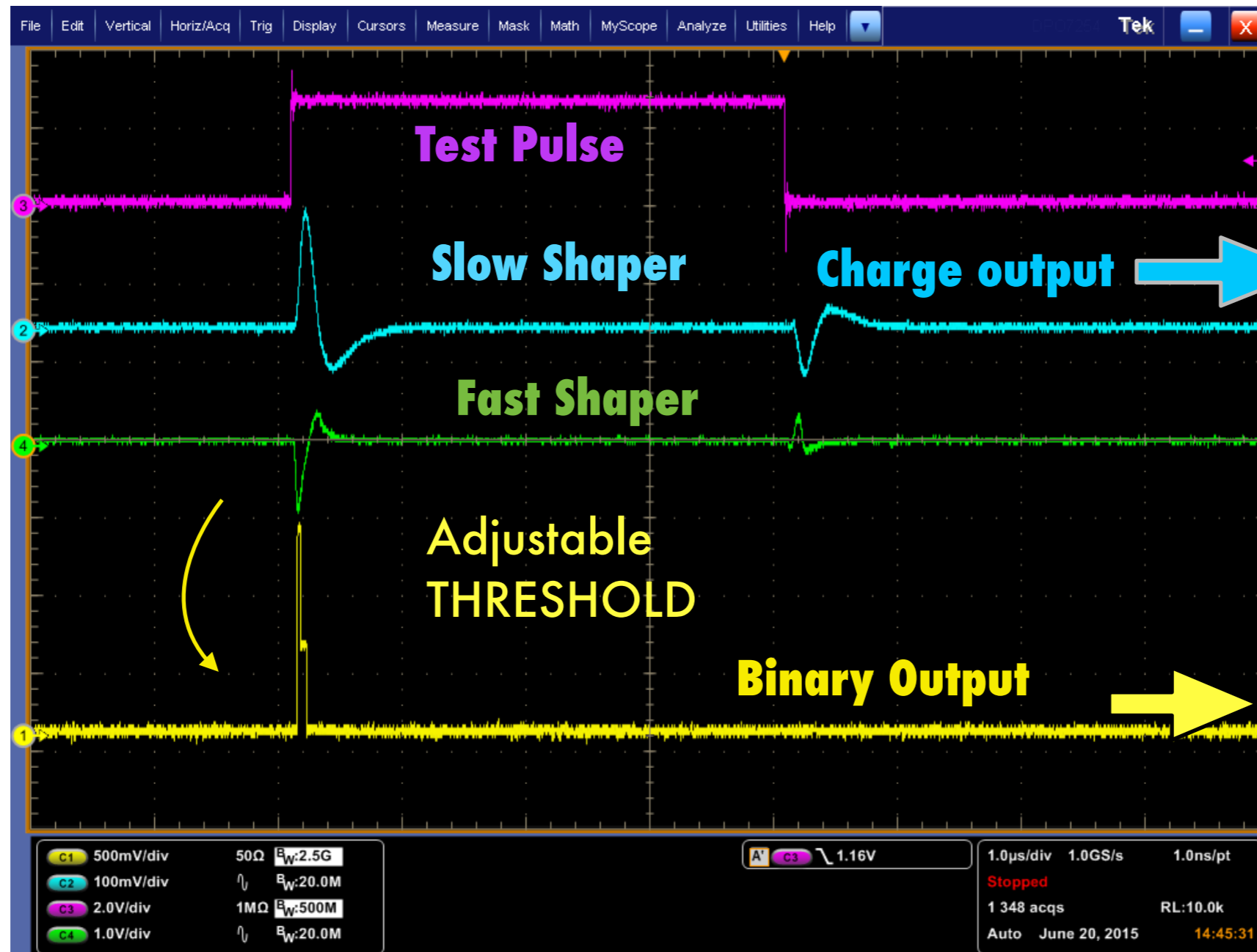
Field Programmable Gate Array (FPGA)Board

- TDC reference clock (1 ns)
- Fixed Latency Trigger (up to 8 μ s)
- MAROC slow controls,
- Stream triggered data to event builder
- Scalers
- FIRMWARE support 192 or 128 channels
- OPTICAL ETHERNET: up to 2.5 Gbps
- TRIGGER MODES: External, Internal, Self (on MAROC binary outputs)



MAROC Signals

example of MAROC signal processing



INPUT
On Board
Test Pulse
1pC

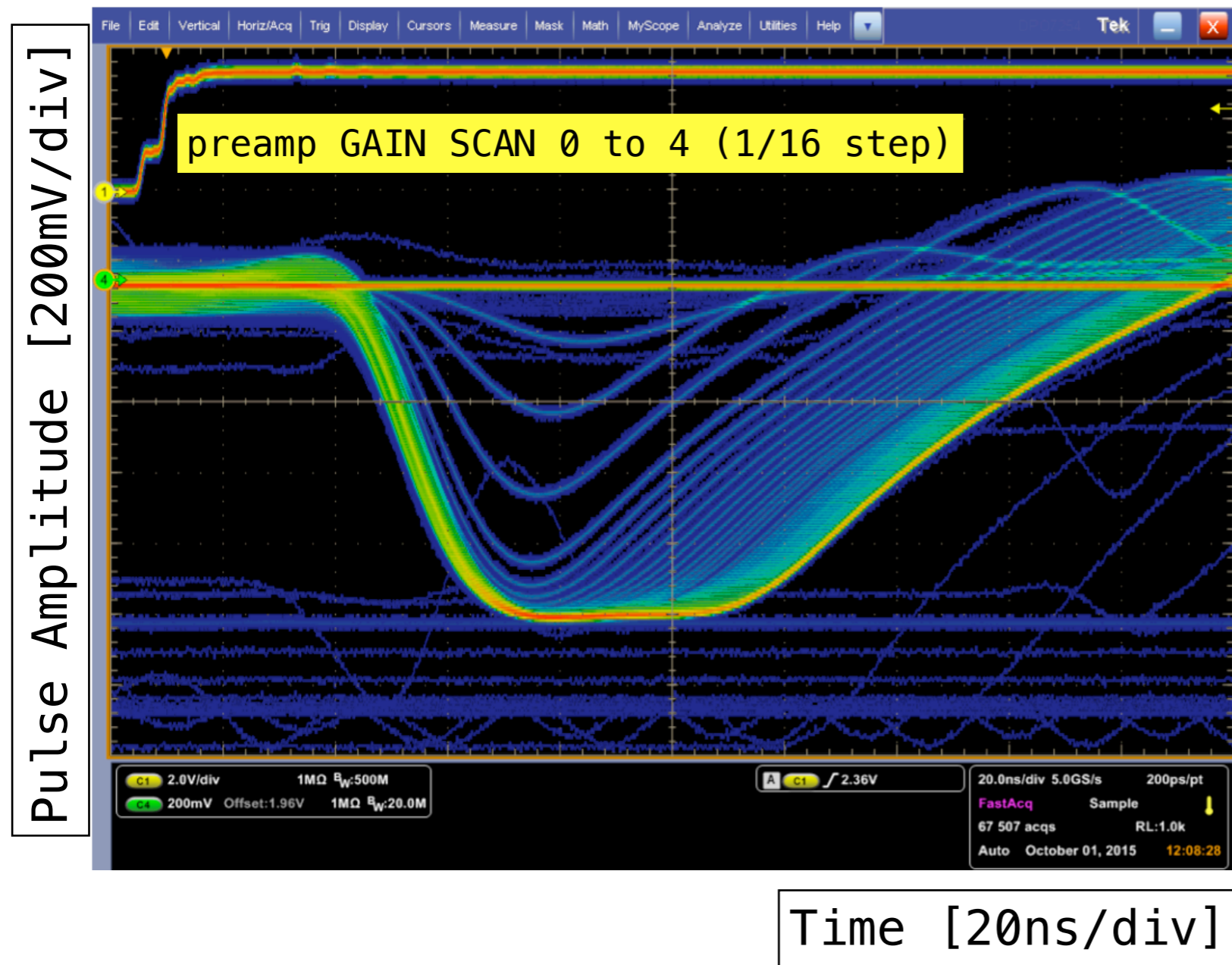
ADC
(MAROC)
calibration only
more on backup slide

SCALER/TDC
(FPGA)

**TDC used for
physics runs!**

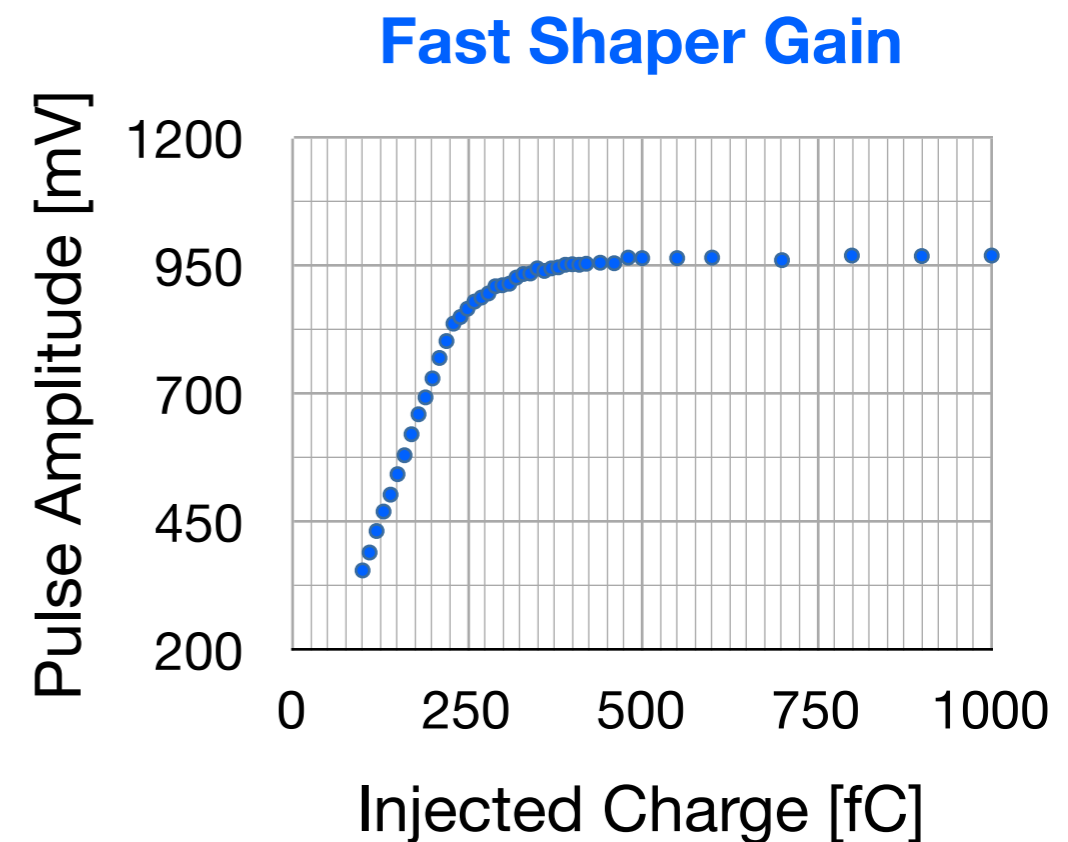
Single channel response, 1 microsecond/div

Gain Scan



Single channel fast shaper response,

High gain shaper
precedes the discriminator
3.75 Volt/pC in the linear region
20-25 ns rise time



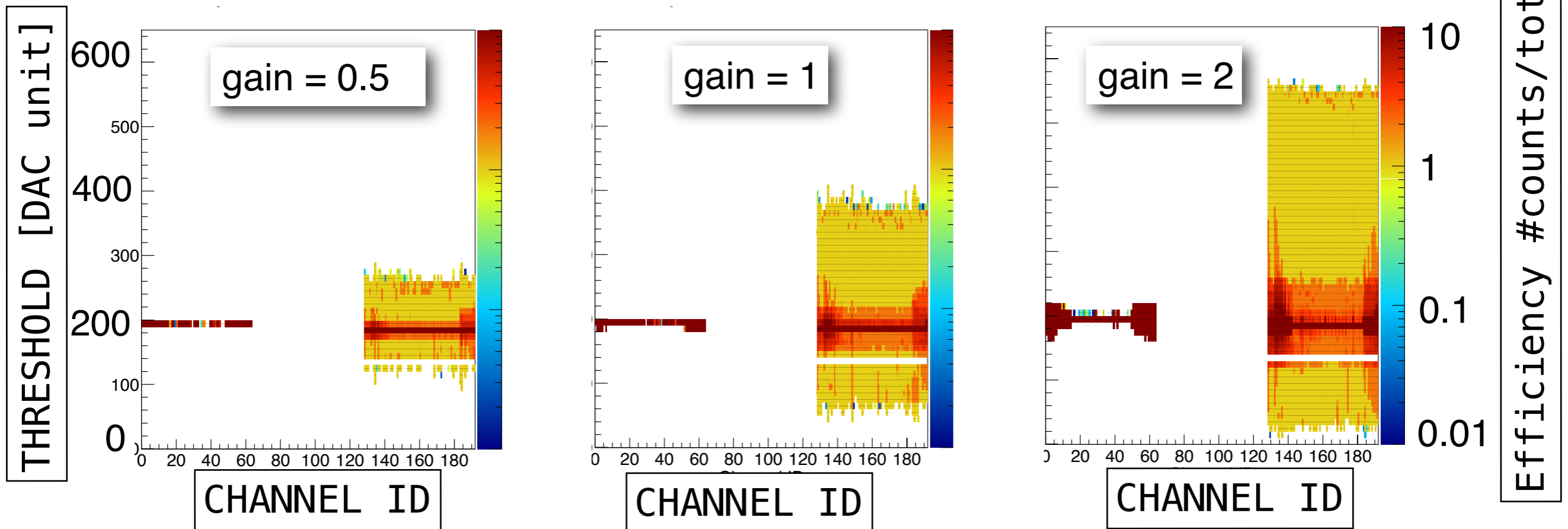
Counting Efficiency Test Pulse

Single photoelectron level (160 fC) 100kHz external pulse generator

128 channels (64 injected, 64 for baseline) **X axis**

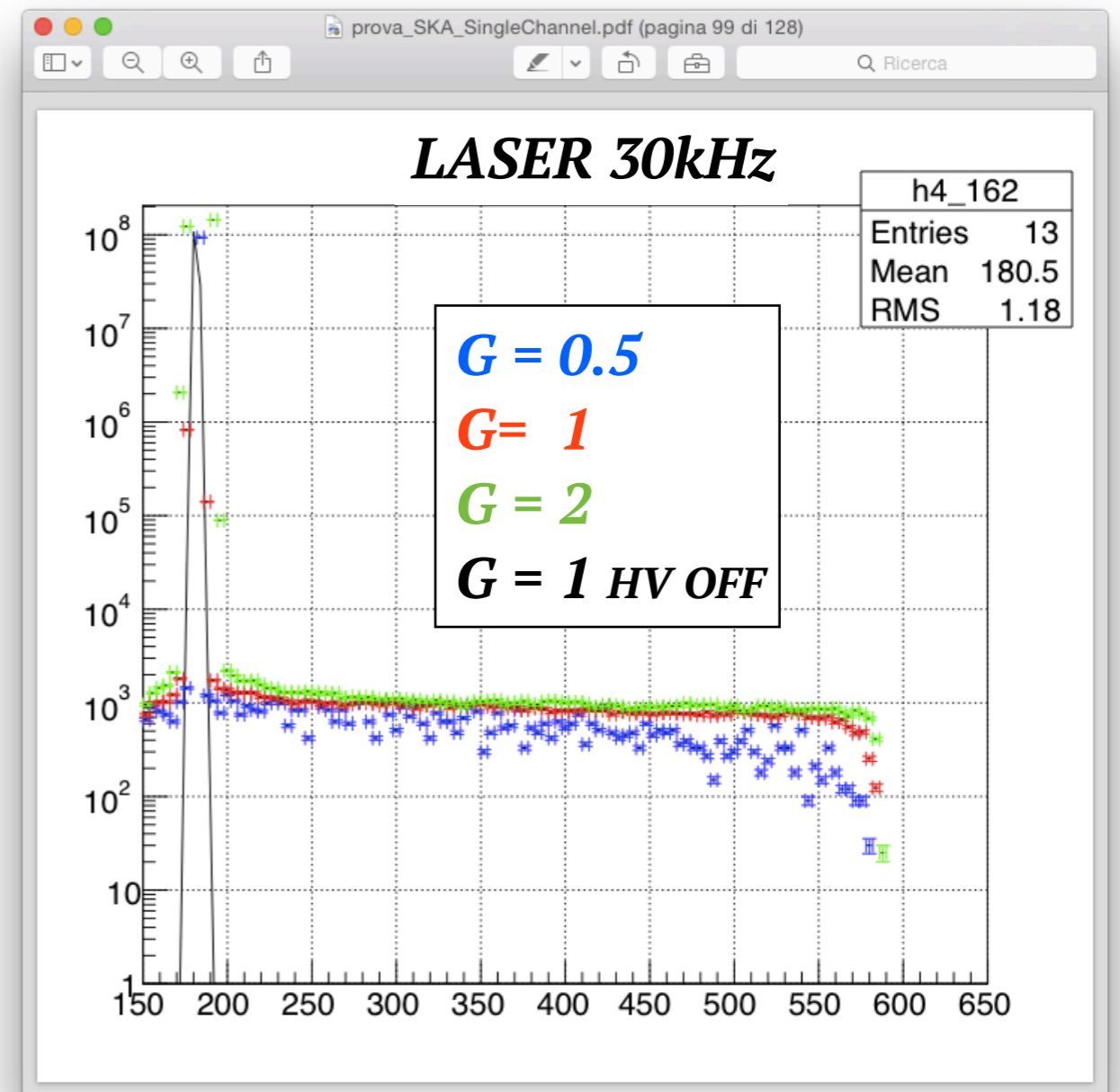
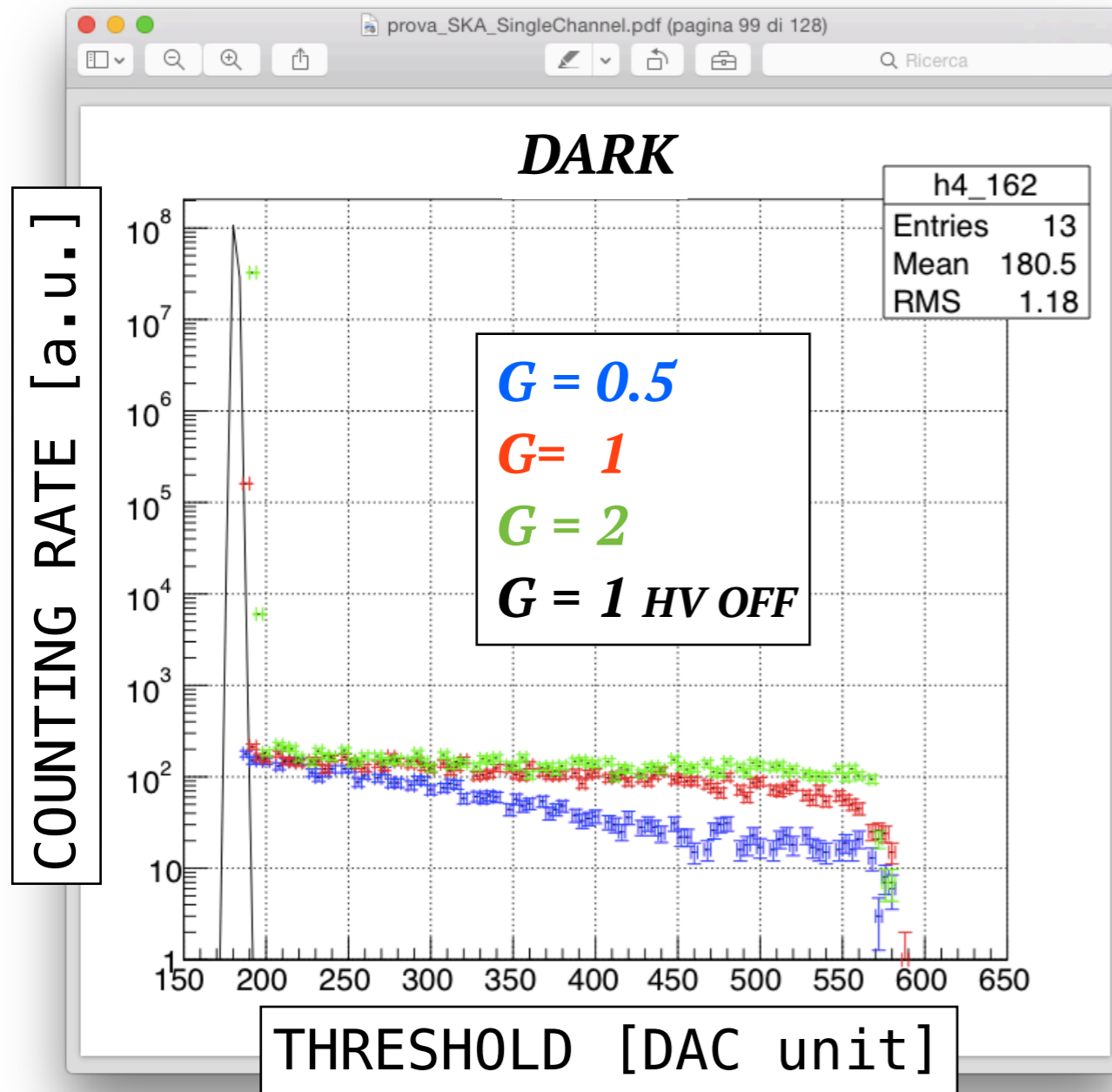
Threshold scan for different preamp gains **Y axis**

Scaler firmware counting **efficiency** (100% inside yellow regions) **Z axis**



Counting Efficiency **Dark & Laser**¹³

Preamp can push low gain pixels to saturation (plateau) allowing an excellent efficiency



Laser at single photoelectron level Hamamatsu

Scaler measurements 30 seconds

H12700 @ 1000 Volts

MA-PMT Dark Rate

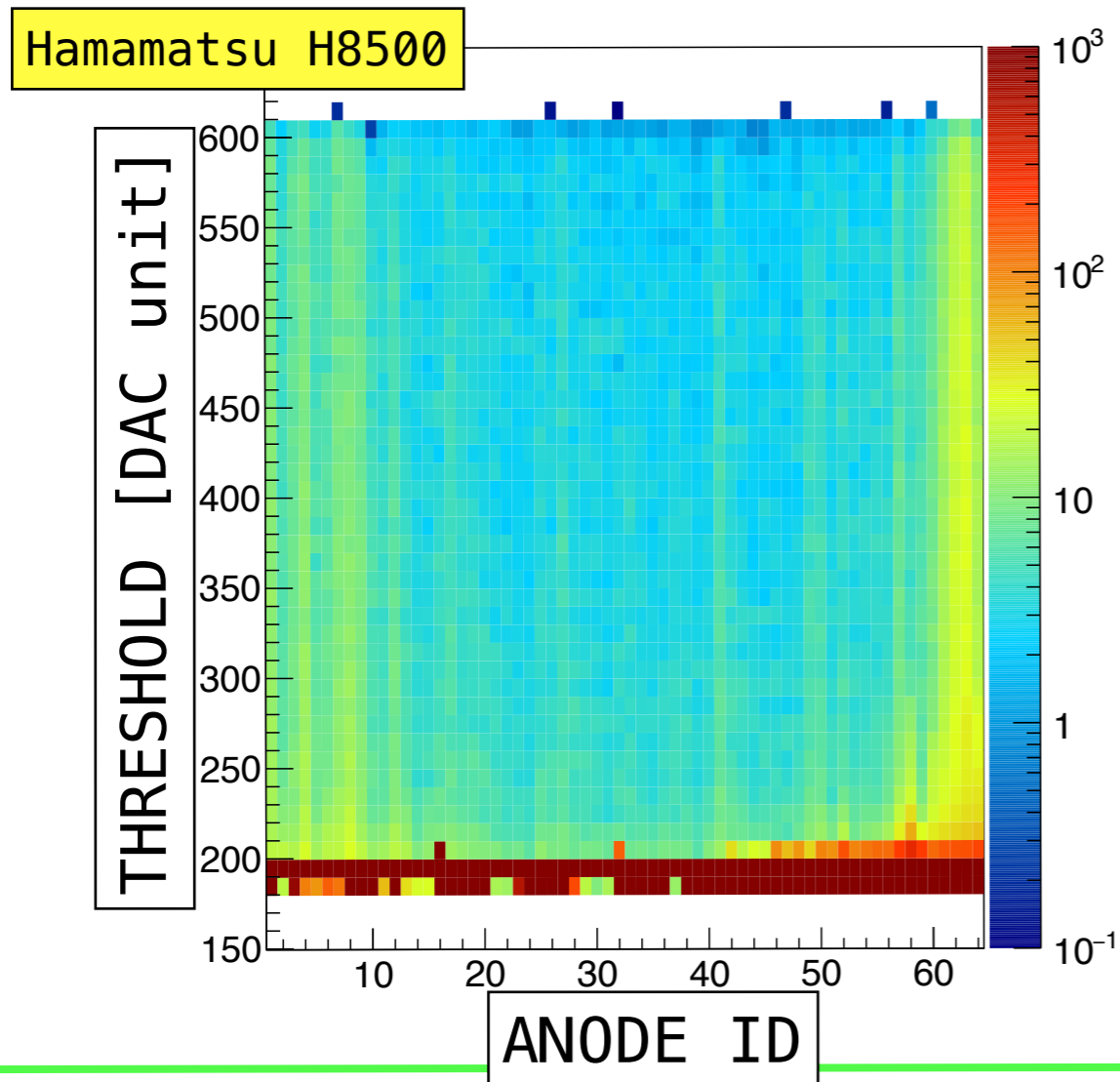
30 seconds scaler measurement

Typical rate
10 Hz/pixel

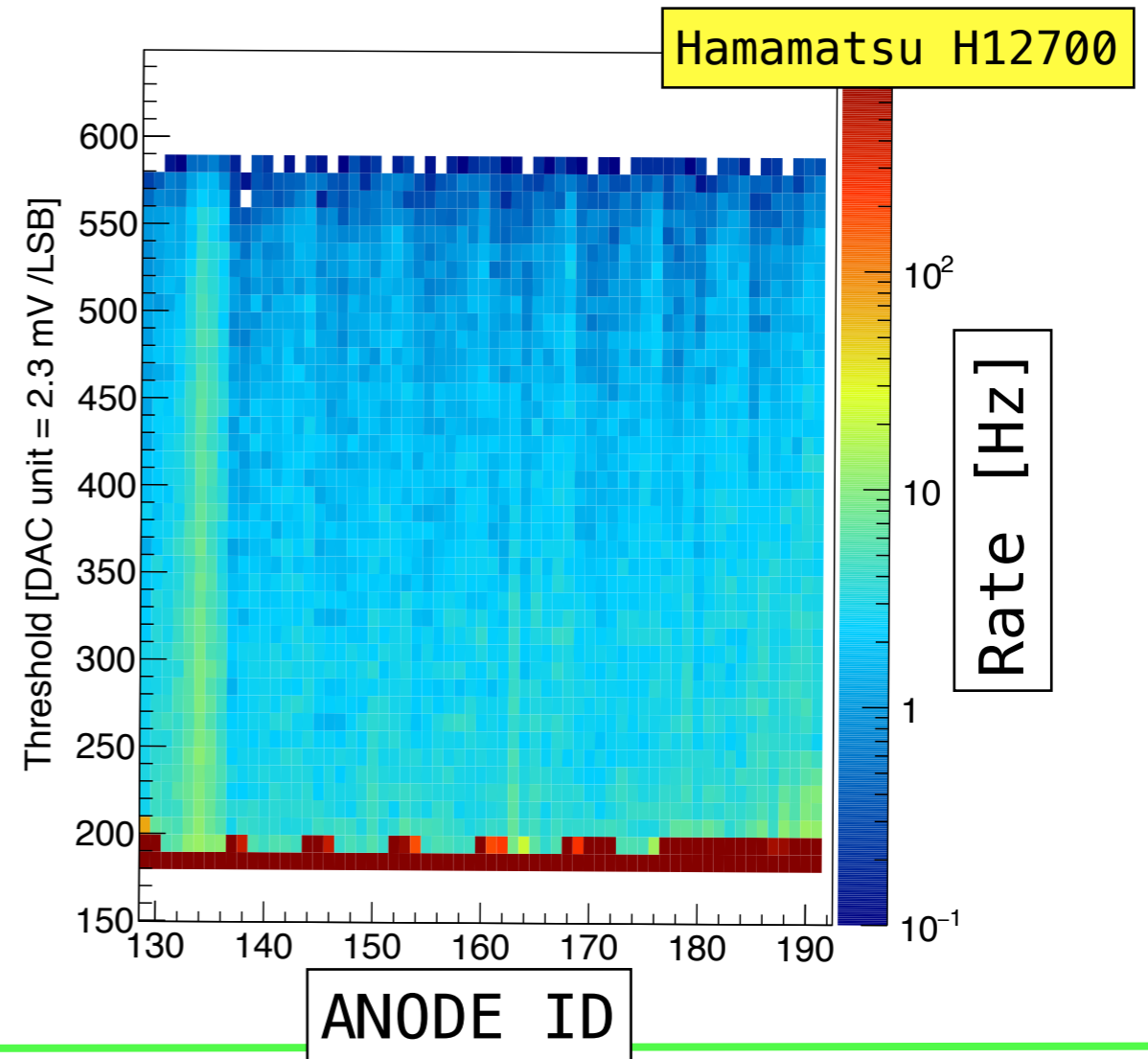


Compatible
with
Hamamatsu
specification

Dark Rate CA7482 HV 1000



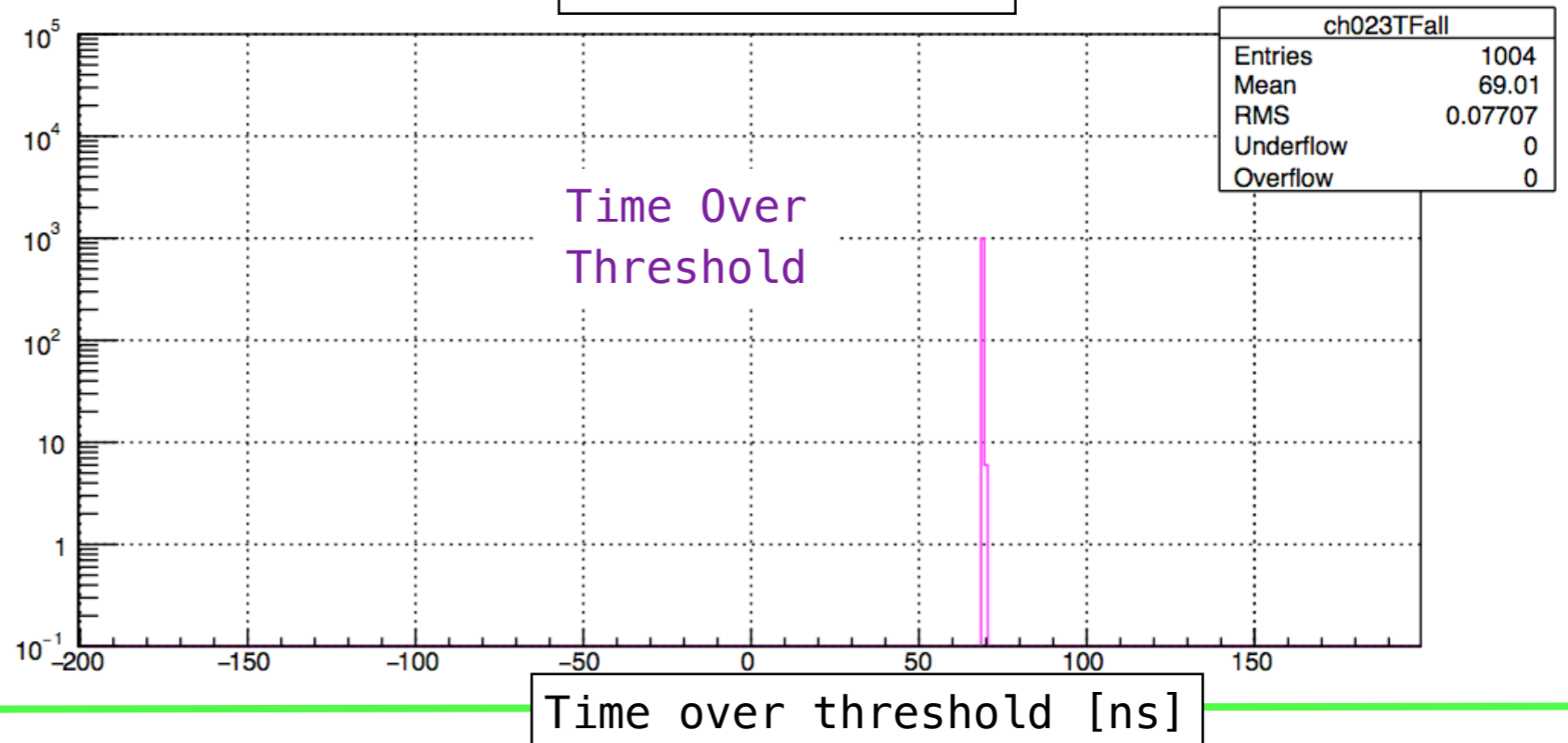
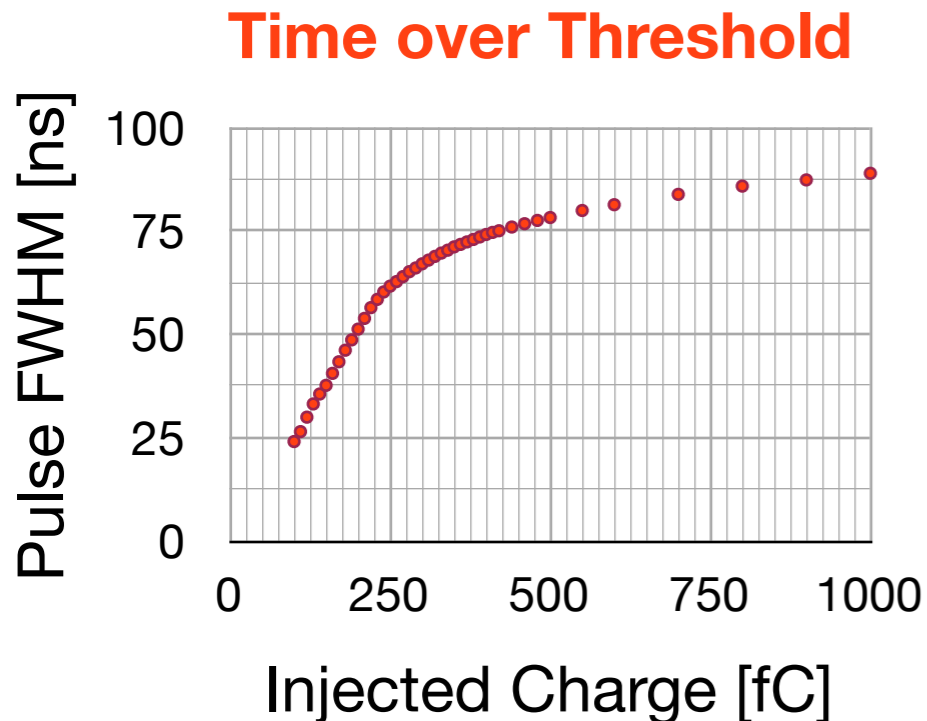
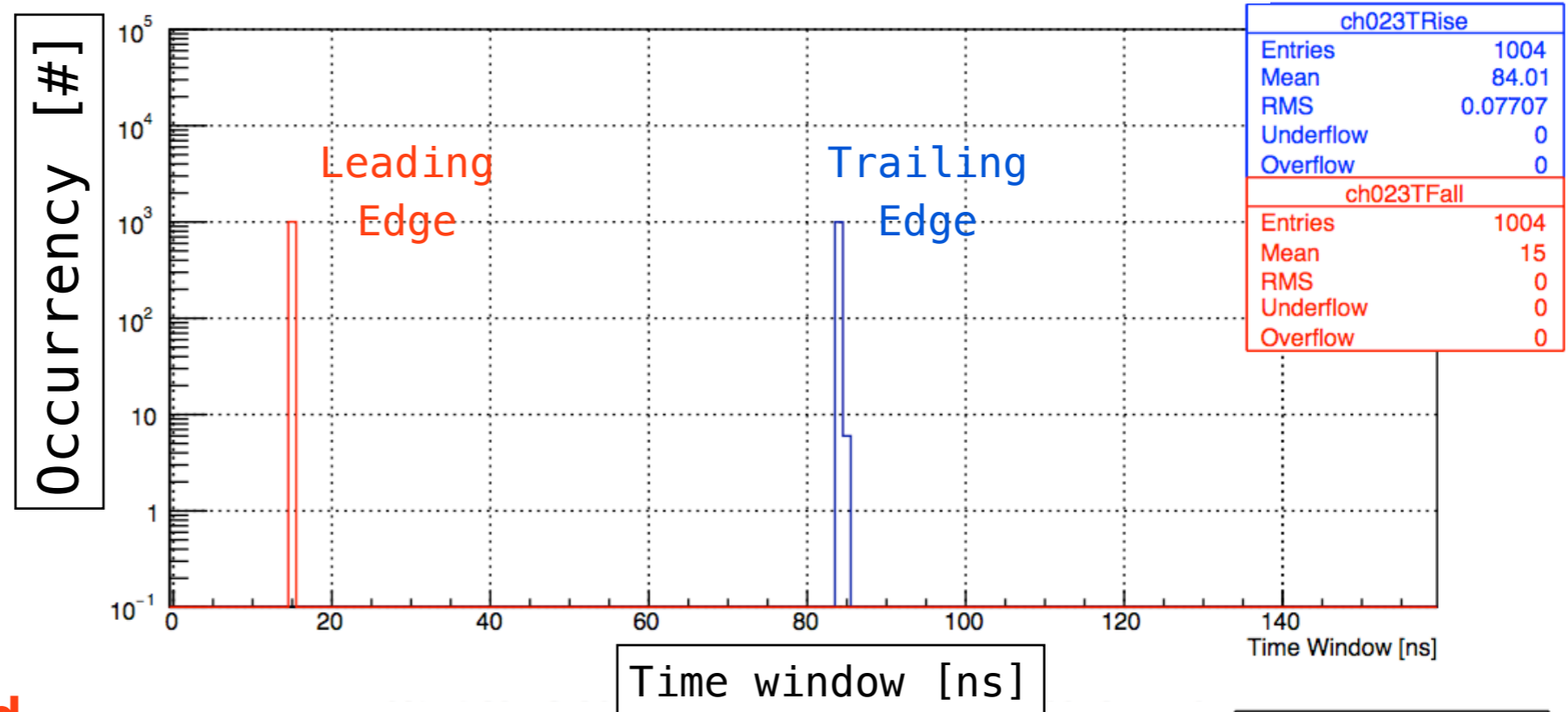
Dark Rate GA0507 HV 1000



TDC Response Test Pulse

Main acquired data are MAROC binary outputs time information

- Jitter introduced by MAROC is below the sensitivity of the TDC (1ns)
- Time over Threshold measurement is feasible



TDC Response Laser + MAPMT

Correlation between leading time and time over threshold (proportional to the charge) allows for time walk correction

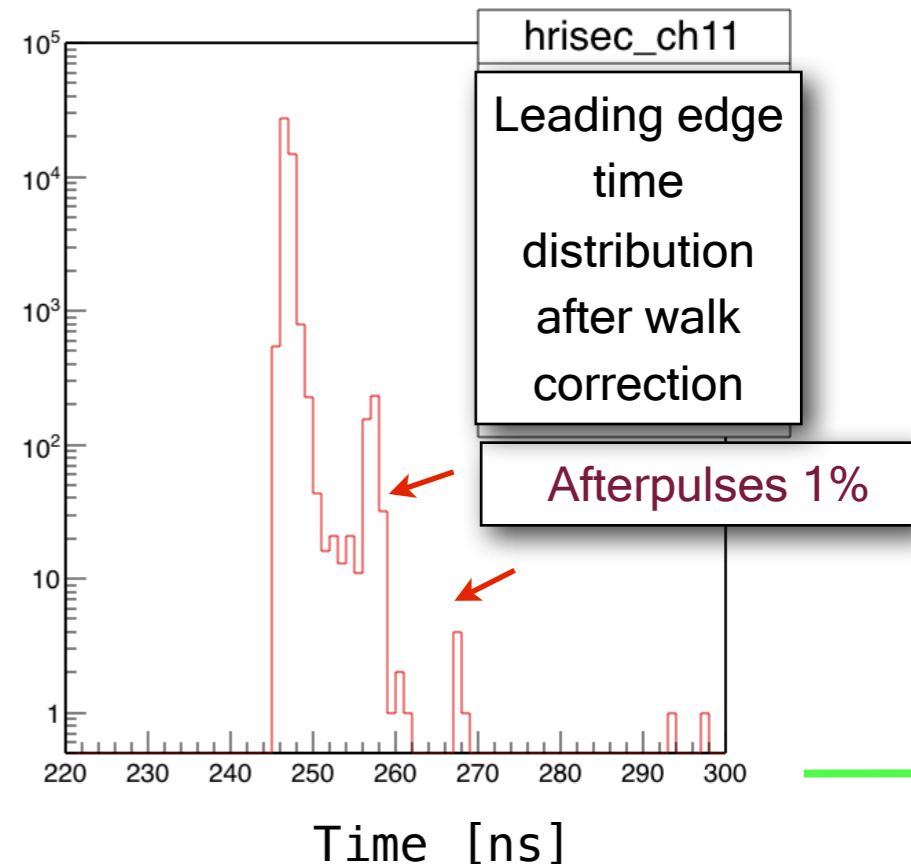
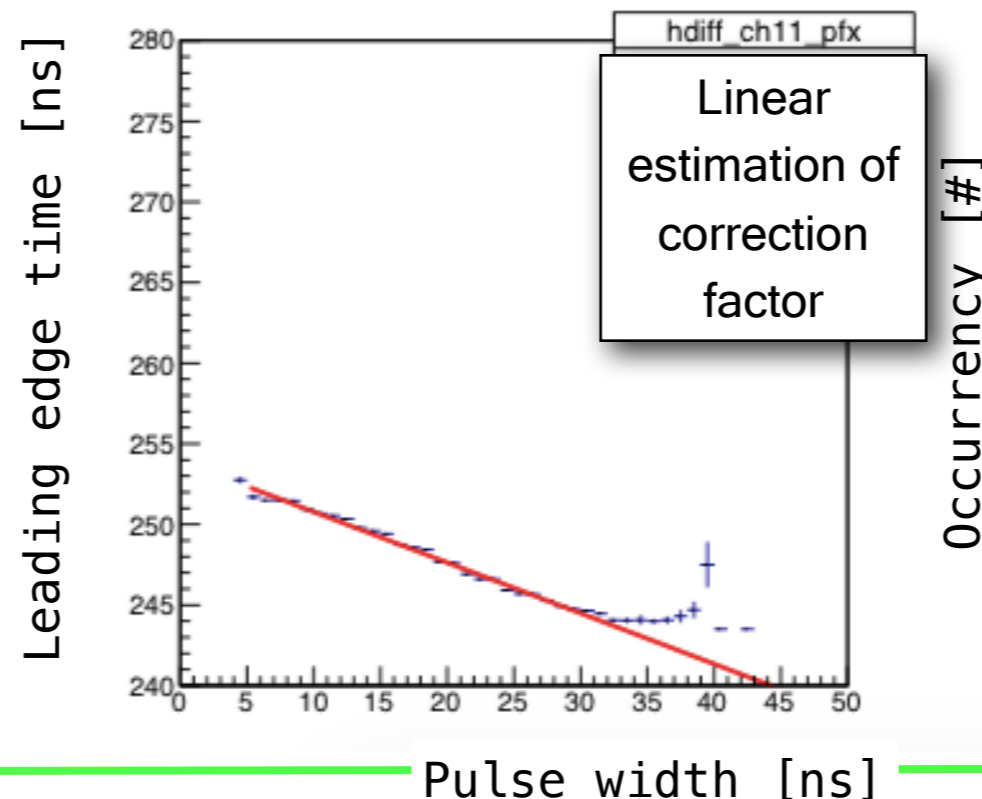
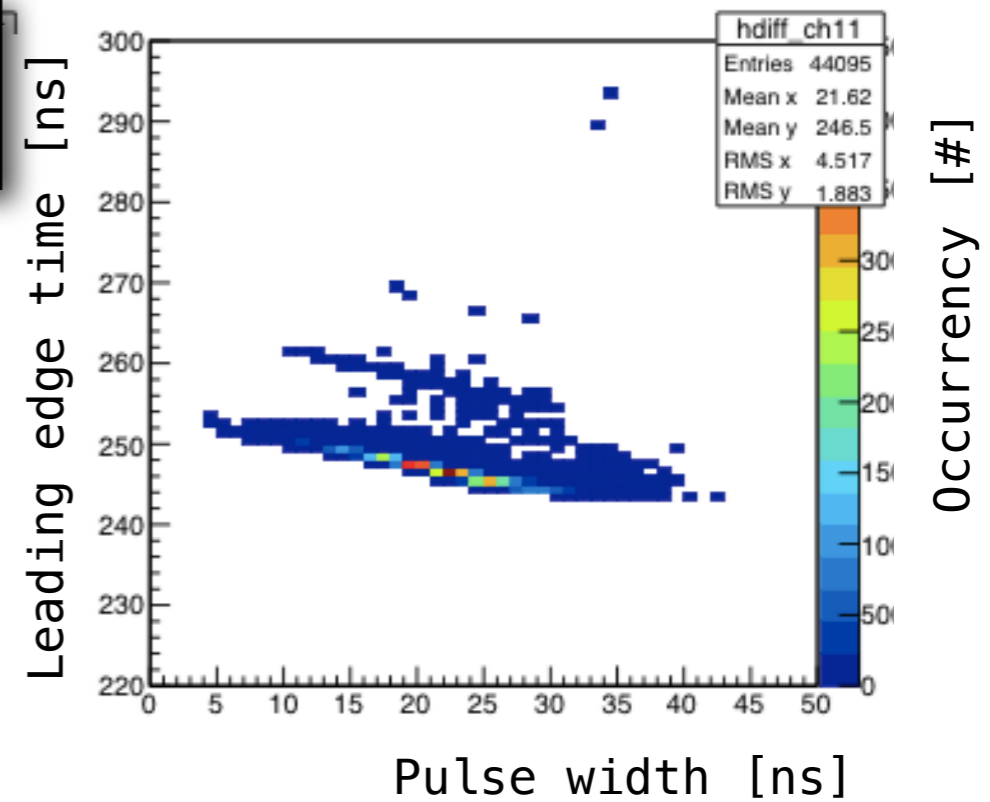
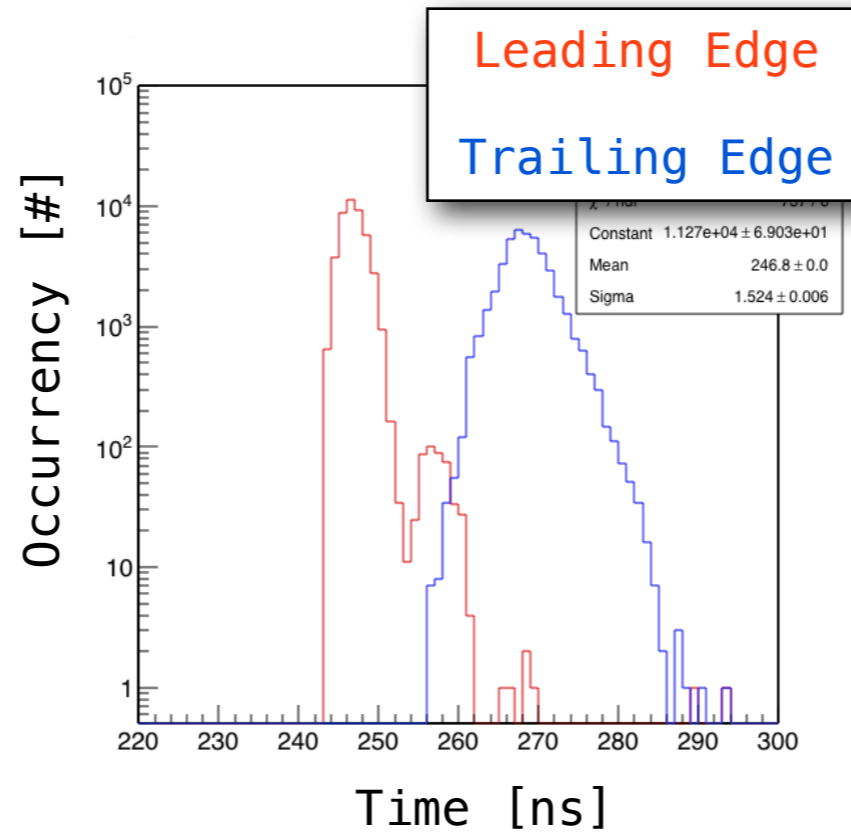
before (top left)

$$\sigma = 1.524 \text{ ns}$$

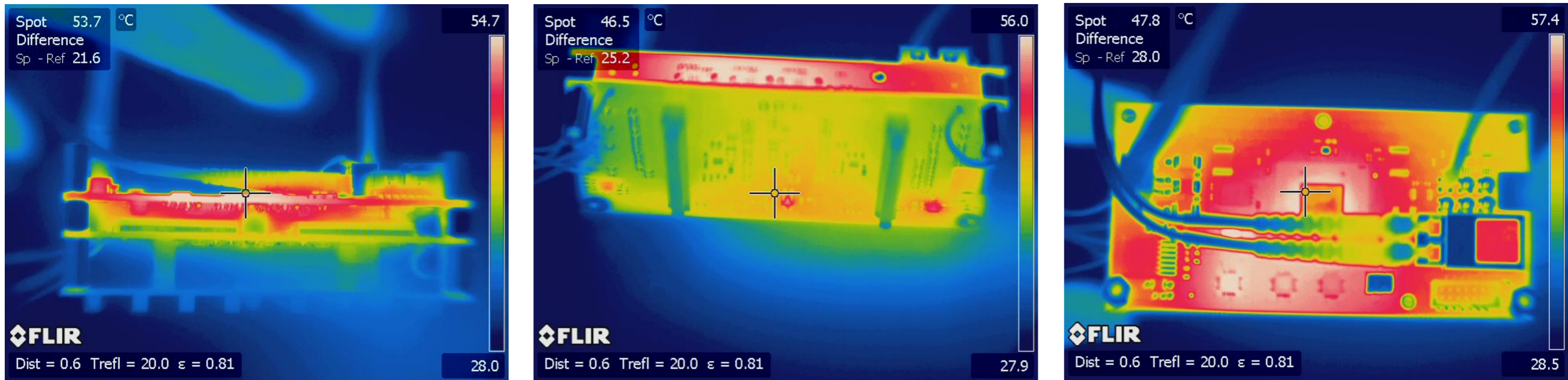
after (bottom right)

$$\sigma = 0.480 \text{ ns}$$

PRELIMINARY



Heat production



Thermographic camera images of a RICH electronic module

- Power Consumption @ 5Volt:

760 mA (3.80 Watts) 3MA-PMTs variant

670 mA (3.35 Watts) 2MA-PMTs variant

Compatible with temperature requirements of CLAS12

Conclusion



CLAS12 RICH will be installed in the JLab Hall B in spring 2017

A compact front end electronics has been developed and tested:

Prototyping (640 channels)

Design validated with test pulse and MA-PMT measurements (Dark and Laser)

Firmware TDC fulfills requirements

Analog MAROC information (internal ADC) will be used for monitoring and debugging

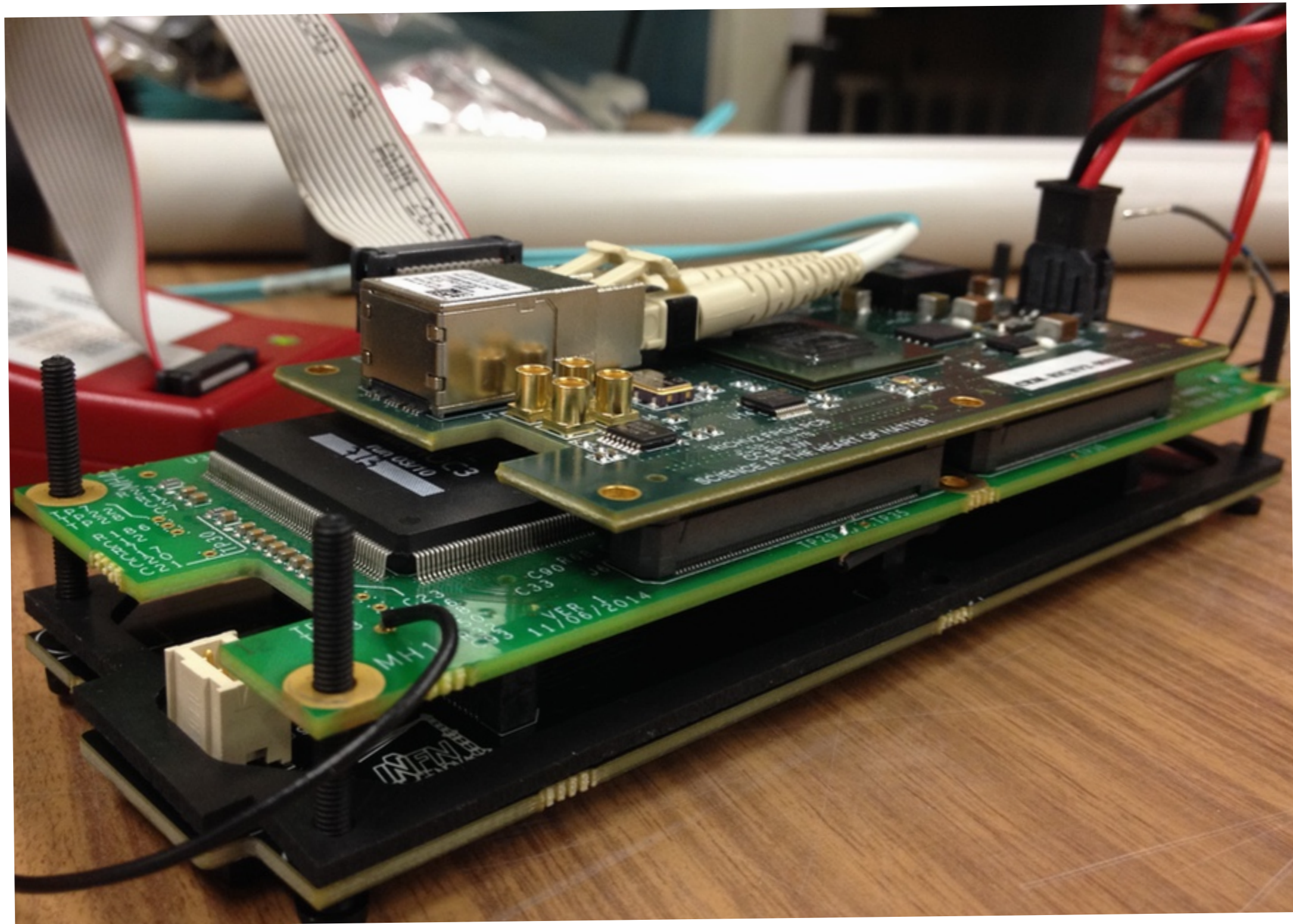
Calibration protocol on study

Production (25000 channels):

Small preproduction (2000 channels) with final optimization introduced during prototyping

Going to full production in 2016

RICH-MAROC Electronics



MAROC internal ADC

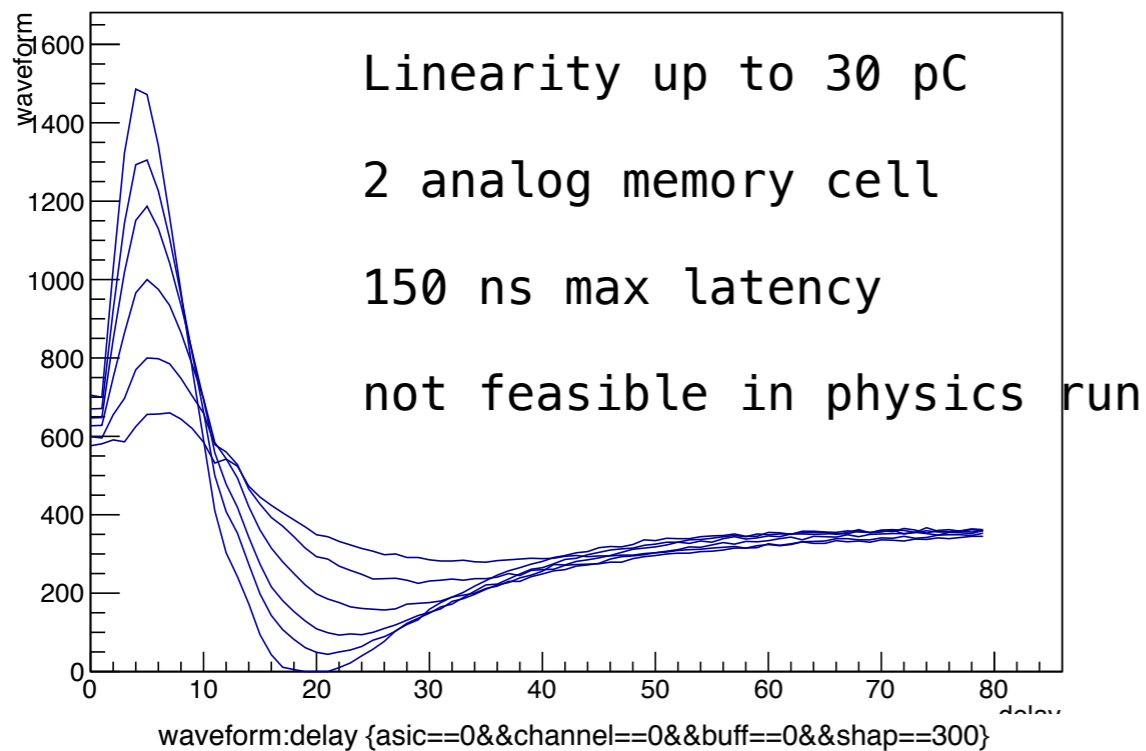
BACKUP SLIDE

Plots: reconstructed waveform using MAROC internal ADC for one channel and different MAROC slow control configurations

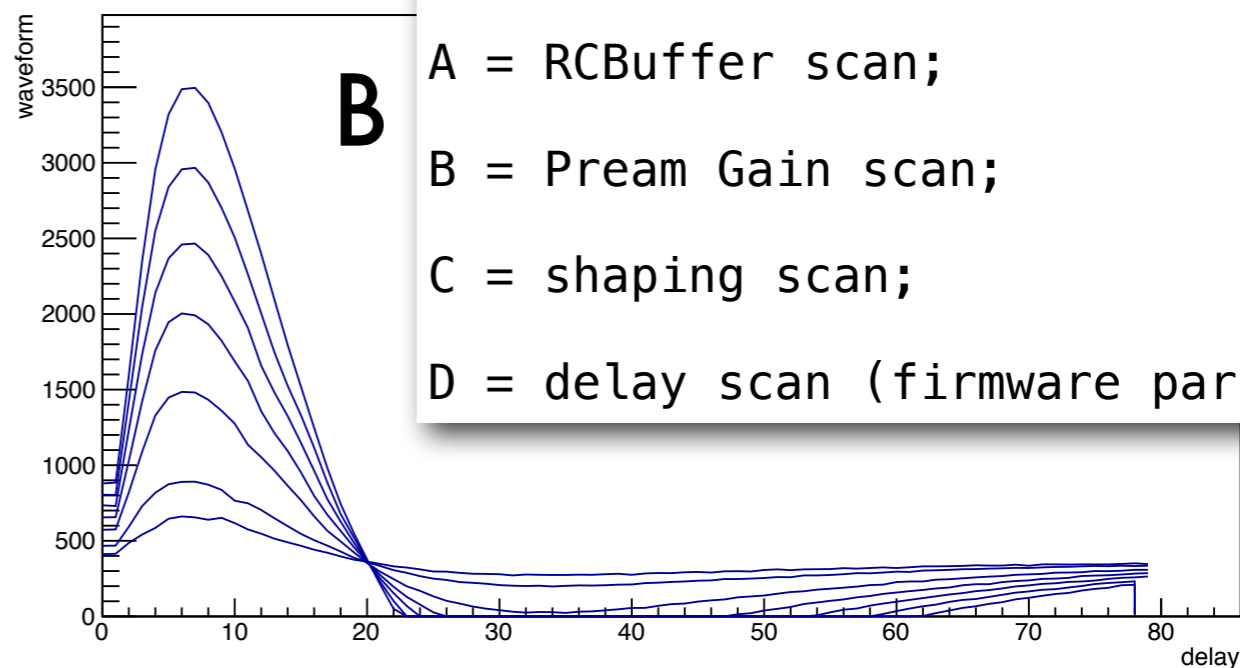
waveform:delay {asic==0&&channel==0&&buff==0&&shap==300}

waveform:delay {

A



B



A = RCBuffer scan;

B = Pream Gain scan;

C = shaping scan;

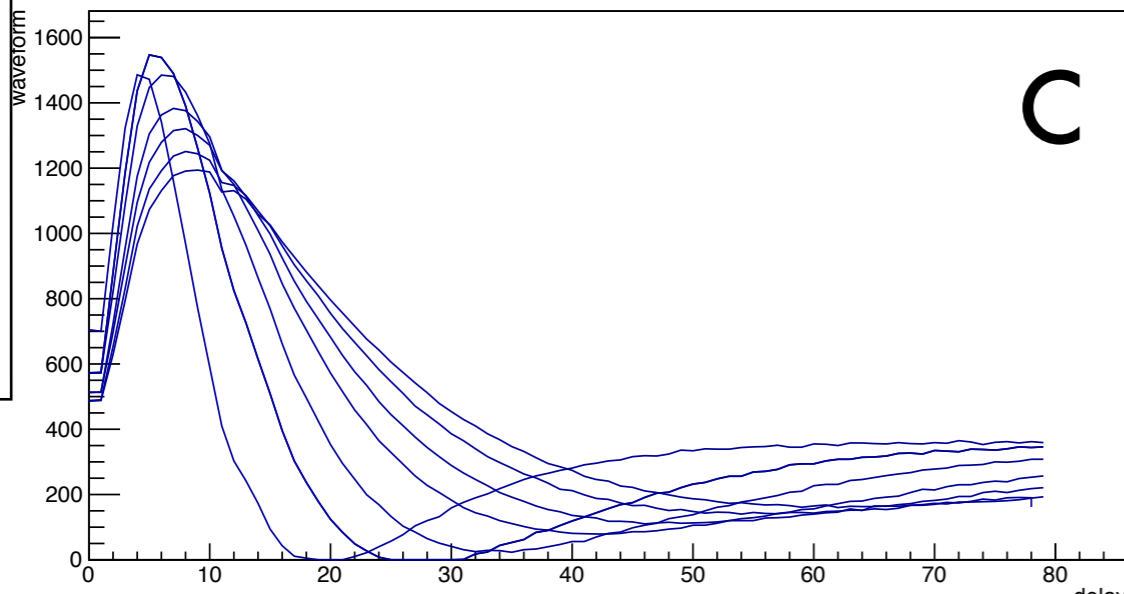
D = delay scan (firmware param)

waveform:delay {asic==0&&channel==0&&buff==0&&shap==300}

adc:delay {asic==0&&channel==0&&trigdelay==50}

Amplitude [ADC units]

C



D

