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A Time-Based Front-End ASIC for the Silicon Micro Strip Sensors of the PANDA Micro Vertex Detector

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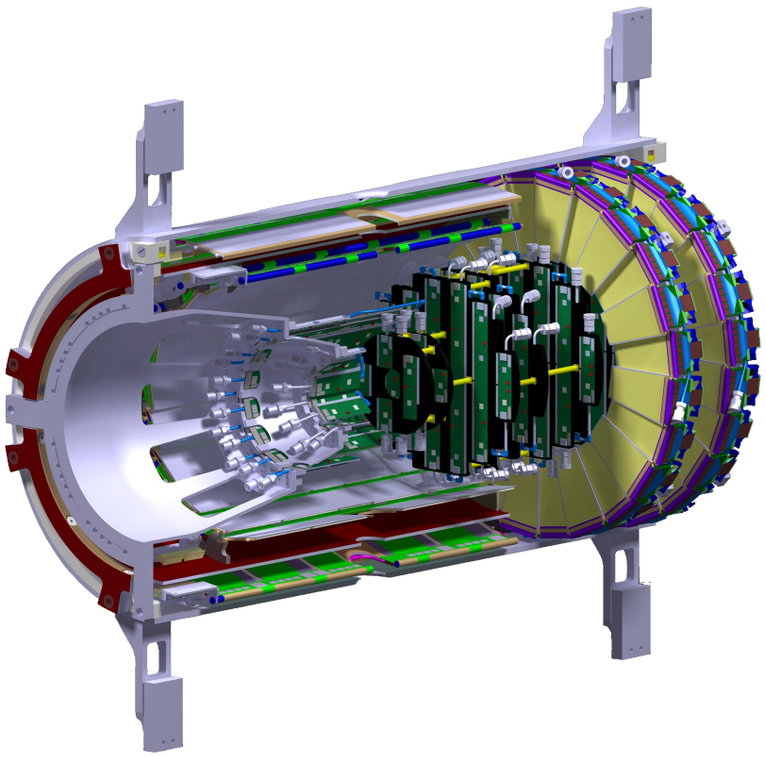
DIRC Workshop 13.11.2015

Contents

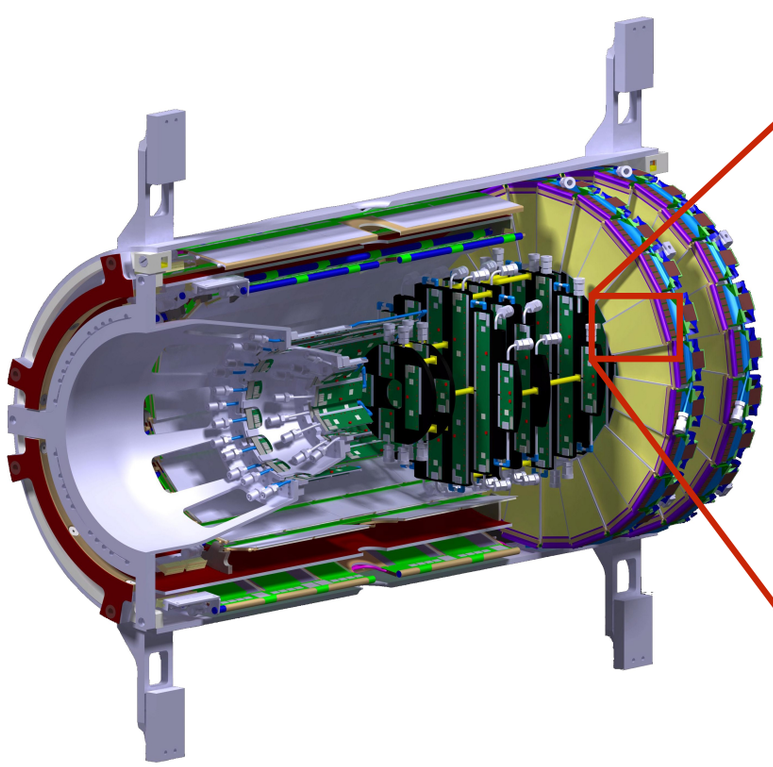
Introduction

Micro Vertex Detector

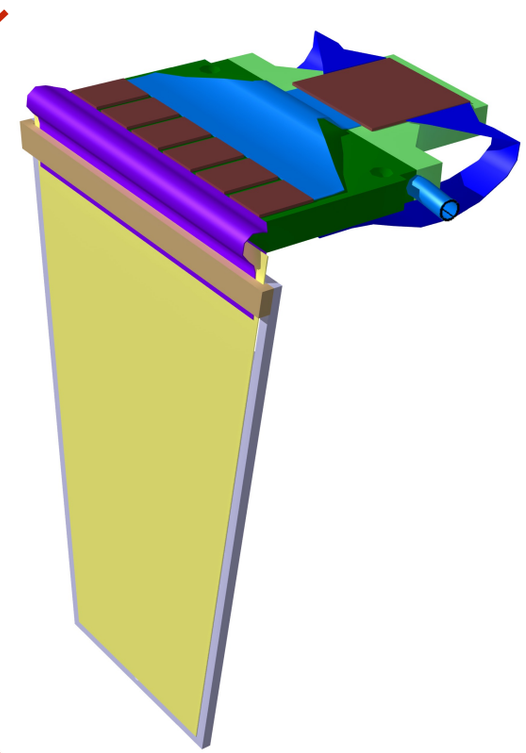


Introduction

Micro Vertex Detector

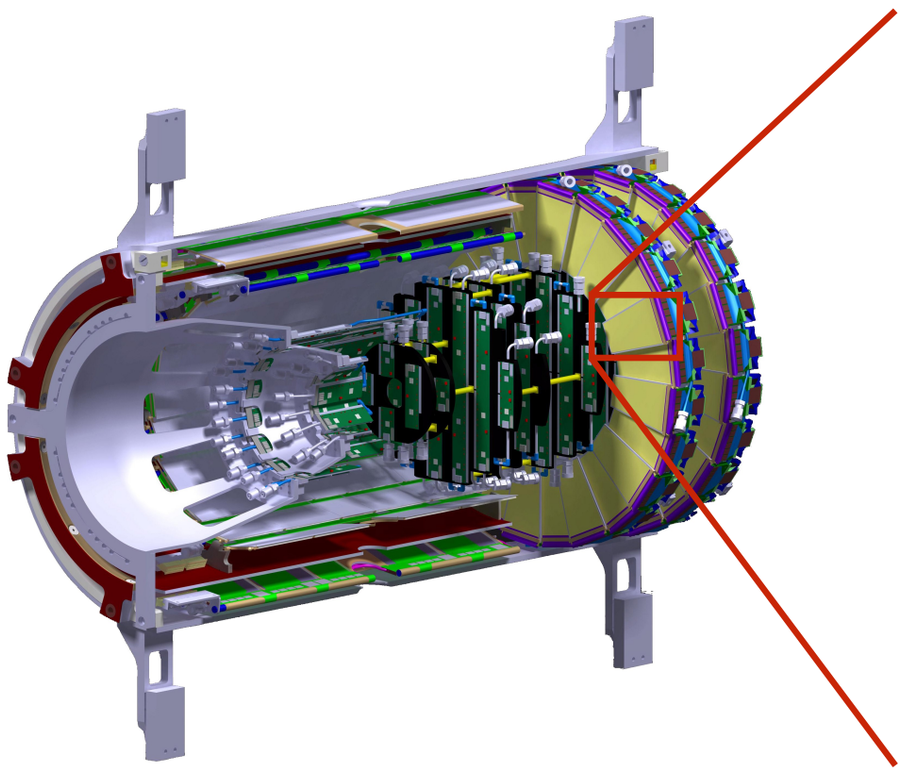


Sensor Module

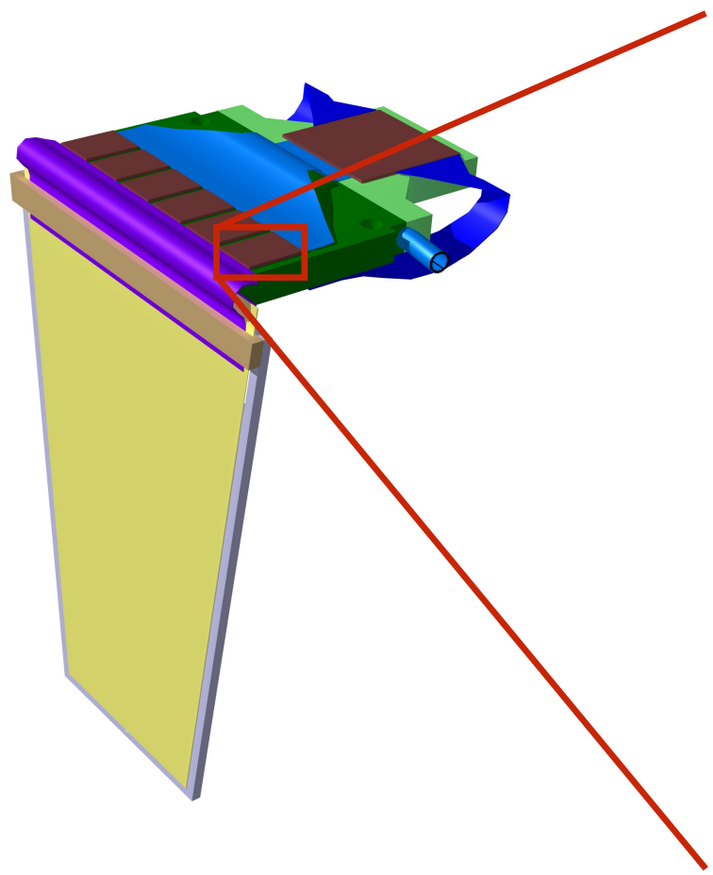


Introduction

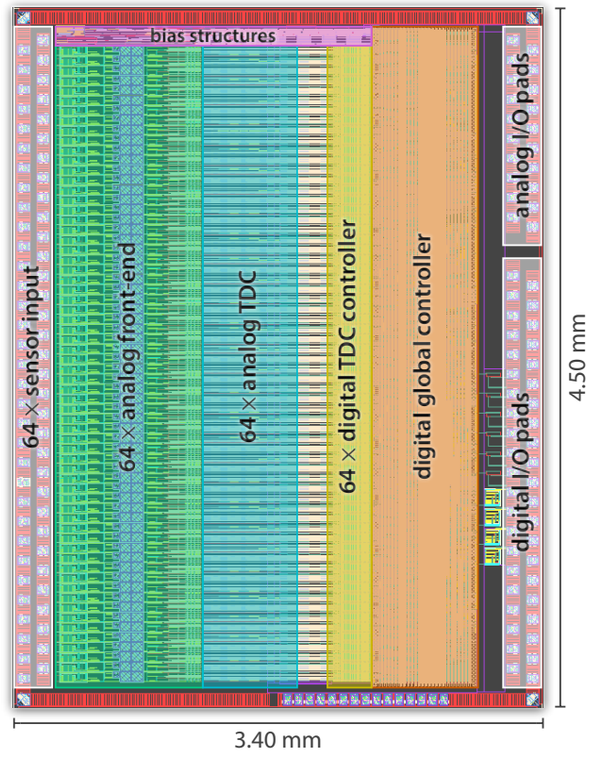
Micro Vertex Detector



Sensor Module



Readout ASIC



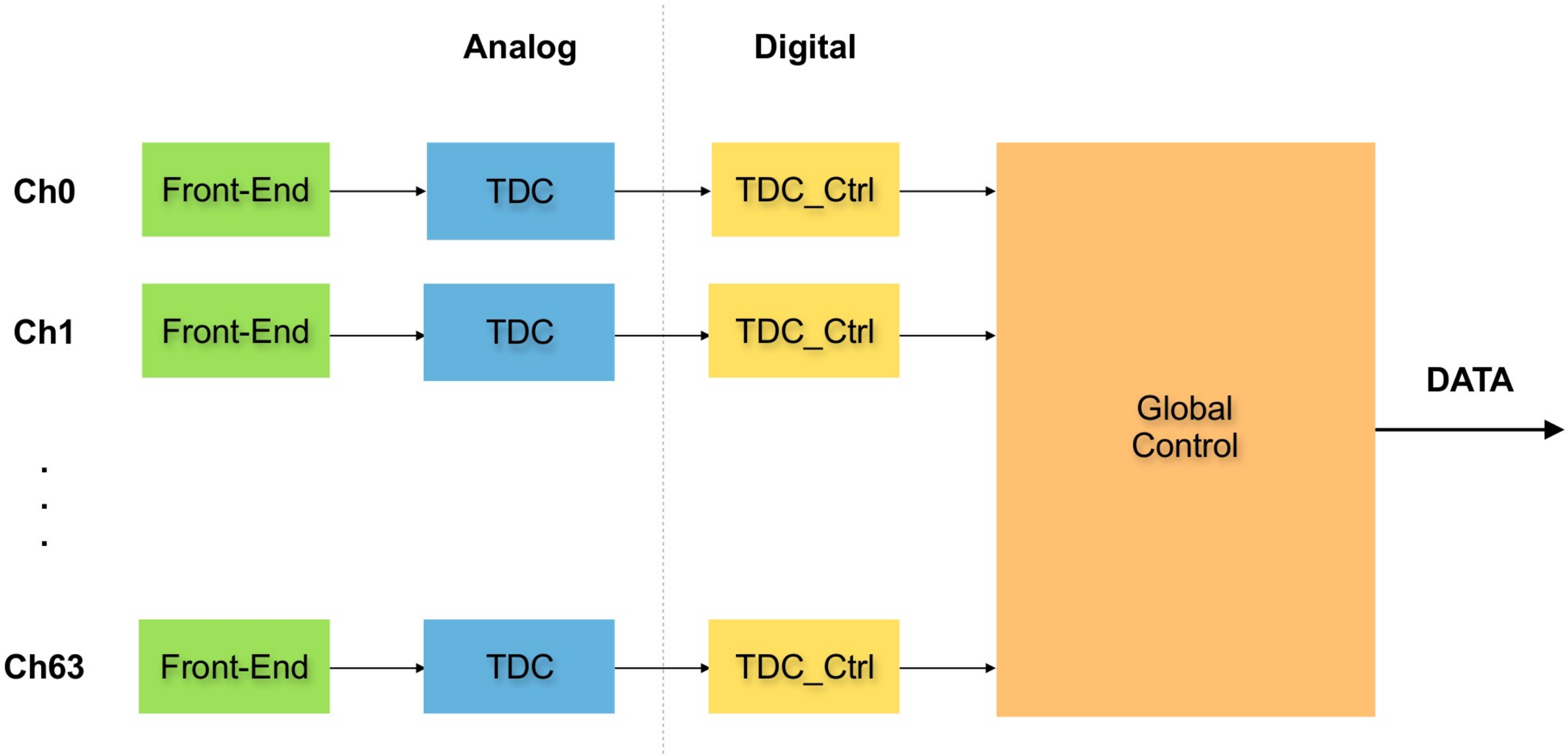
PANDA Strip ASIC

Key features

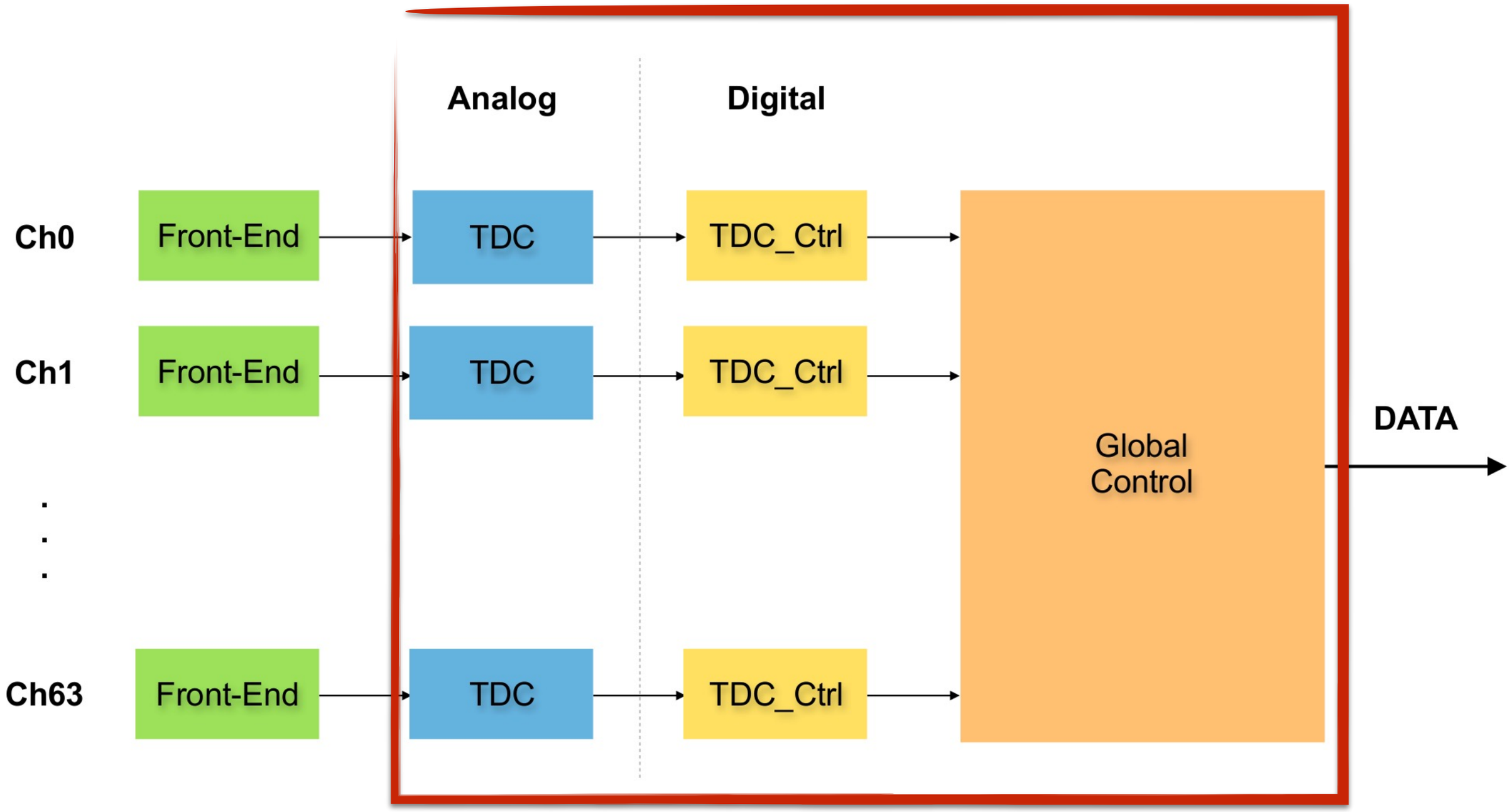
Channels	64
Input pitch	63 µm
Rate capability	100 kHz/channel
Power consumption	< 4 mW/channel
Front-end noise	< 600 e^-
Time bin width	50 - 400 ps
Charge resolution	8 bit (dyn. range) *
Radiation tolerance	100 kGy *

* Design goal

ASIC Architecture

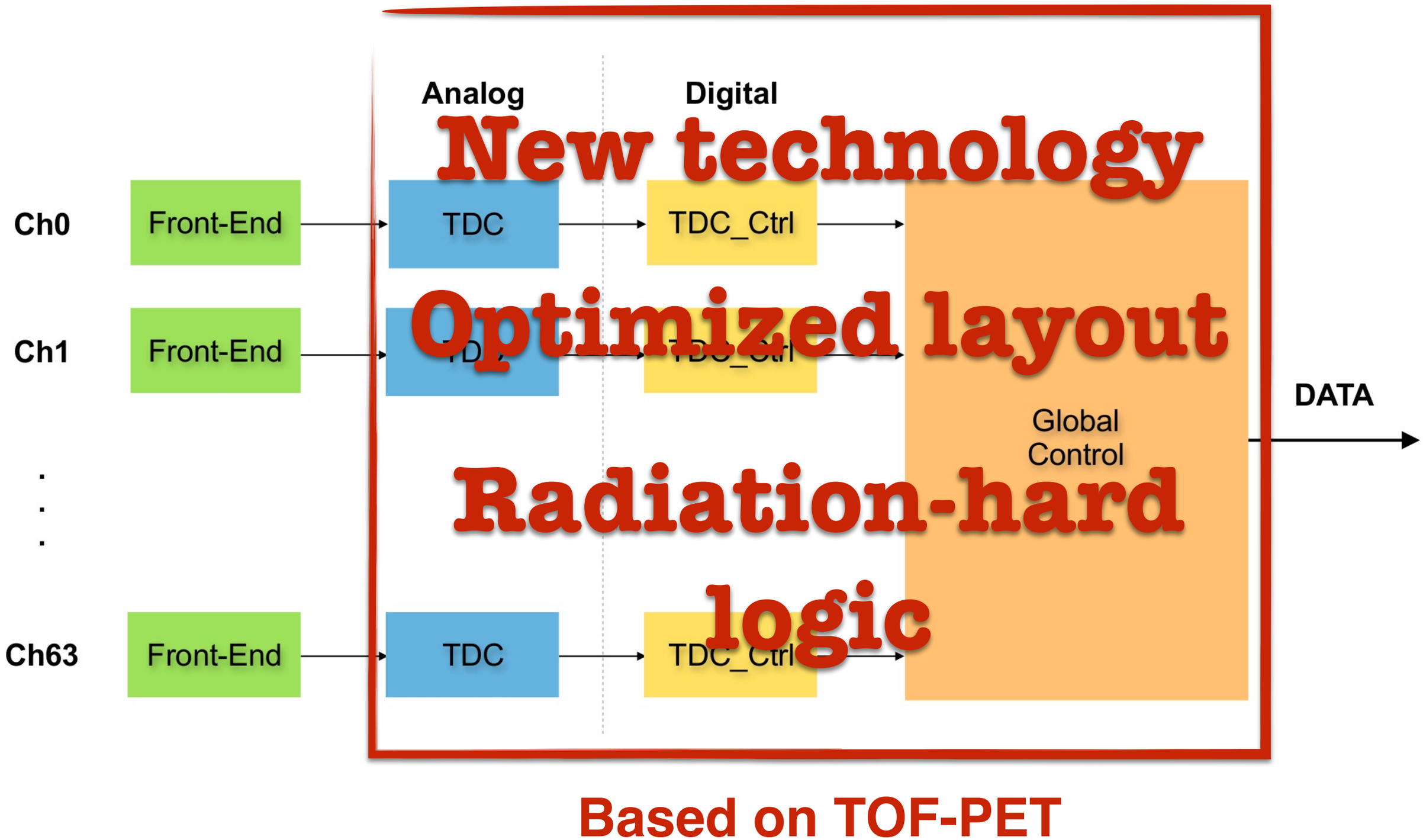


ASIC Architecture

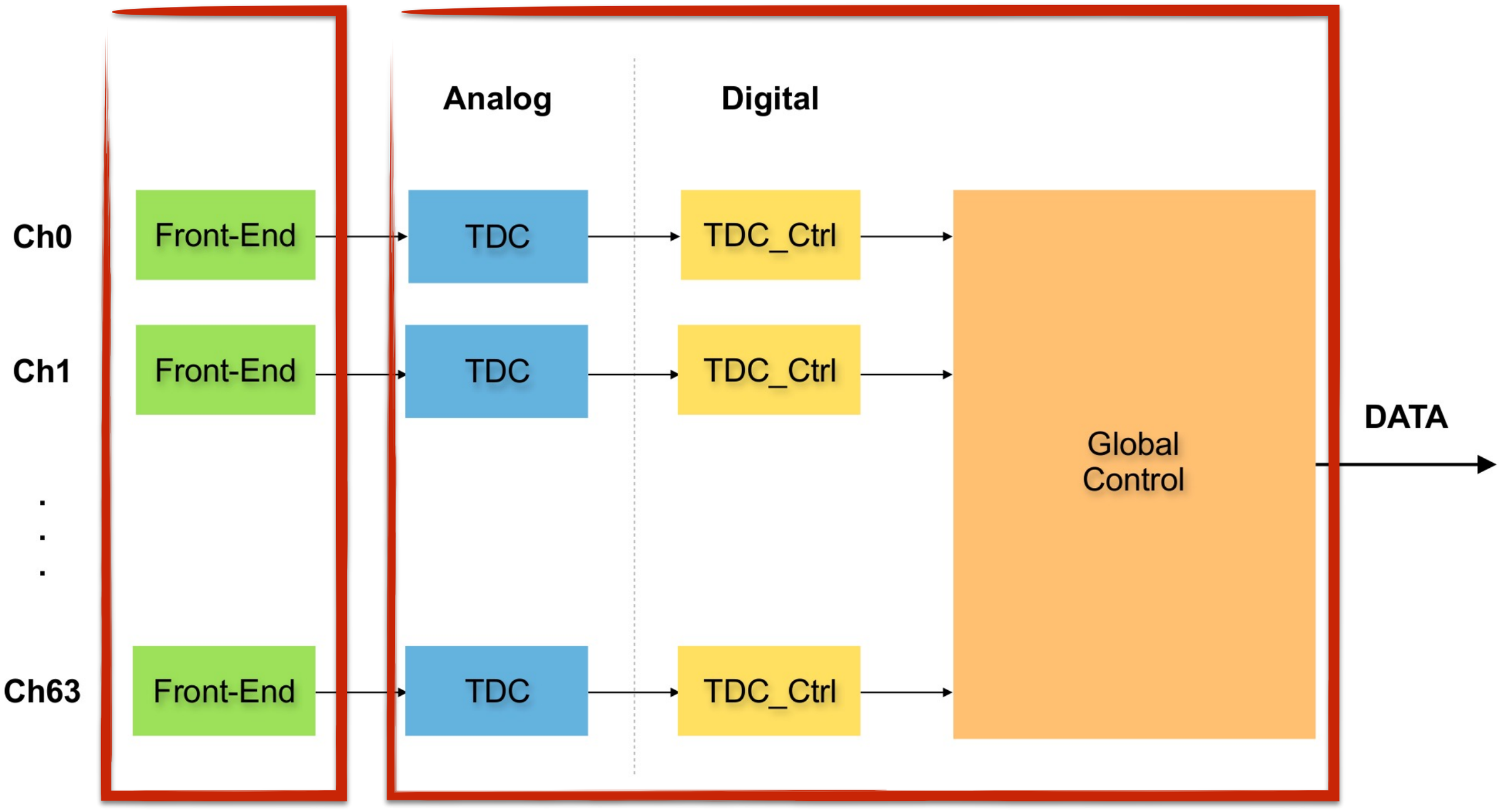


Based on TOF-PET

ASIC Architecture

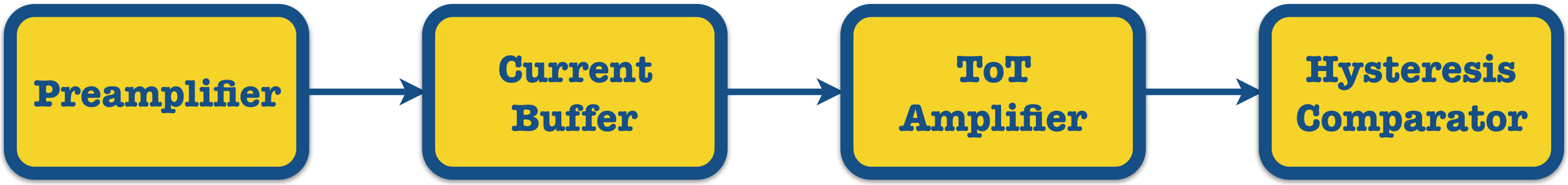


ASIC Architecture

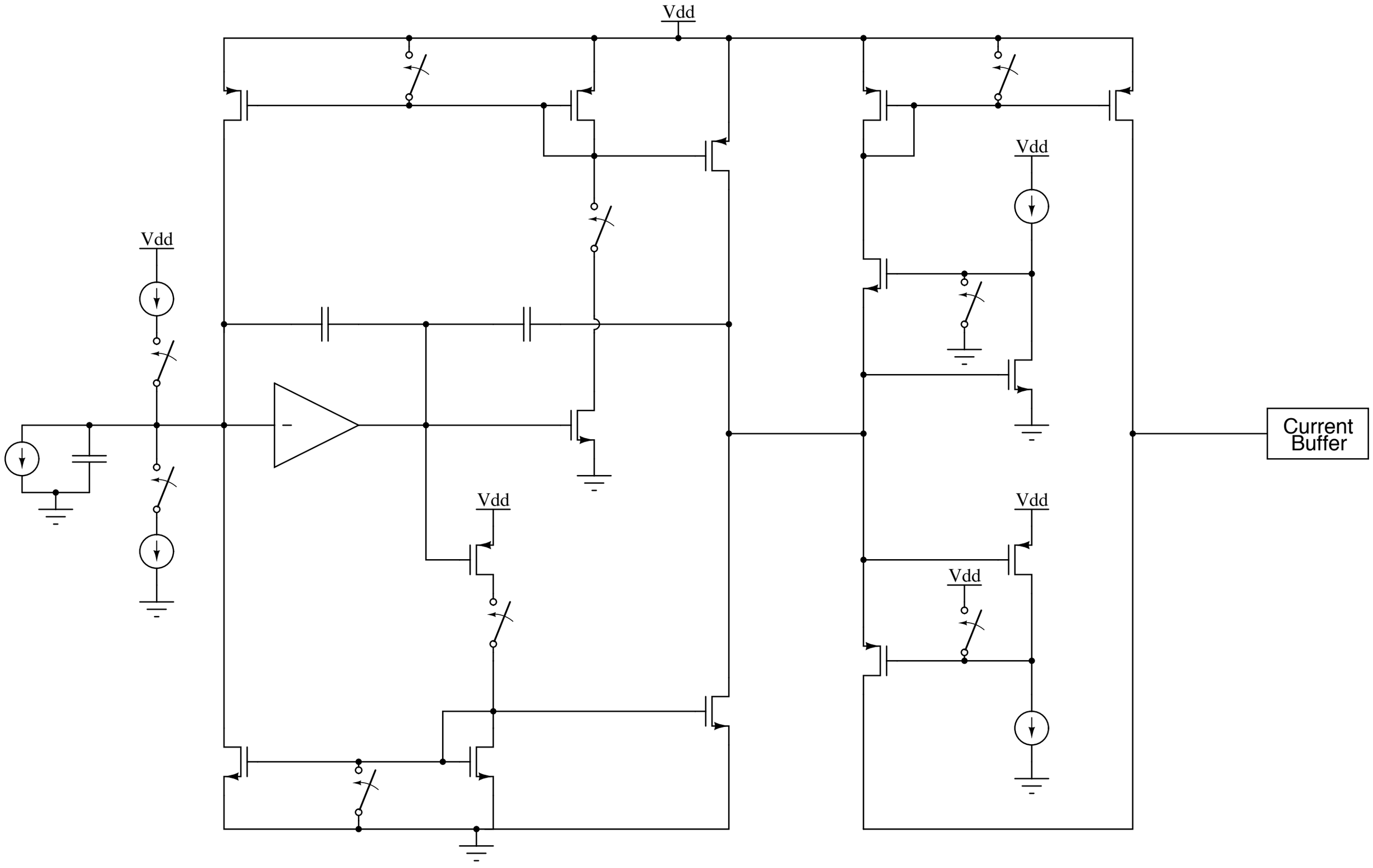


New design **Based on TOF-PET**

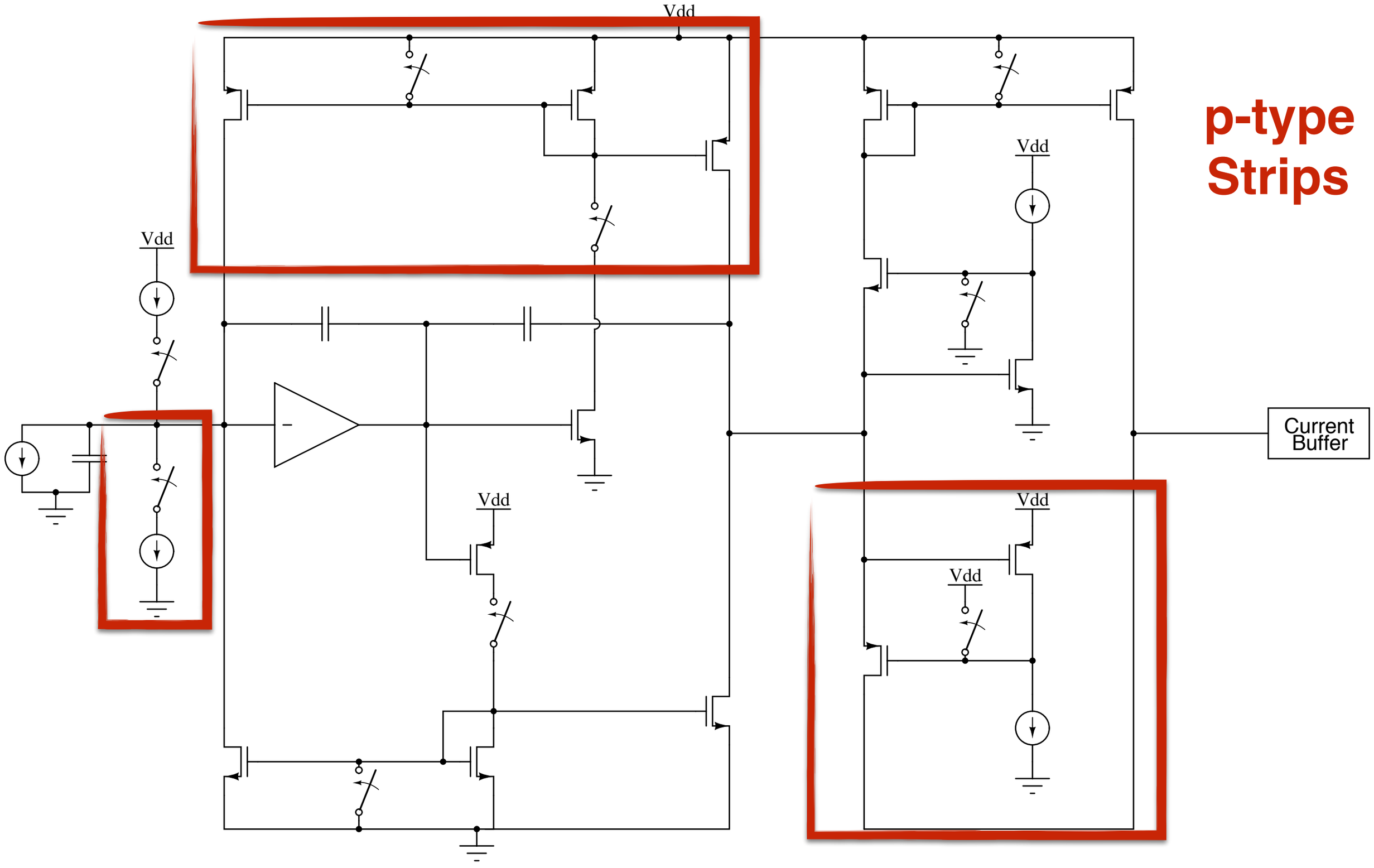
Front-End Amplifier



Preamplifier

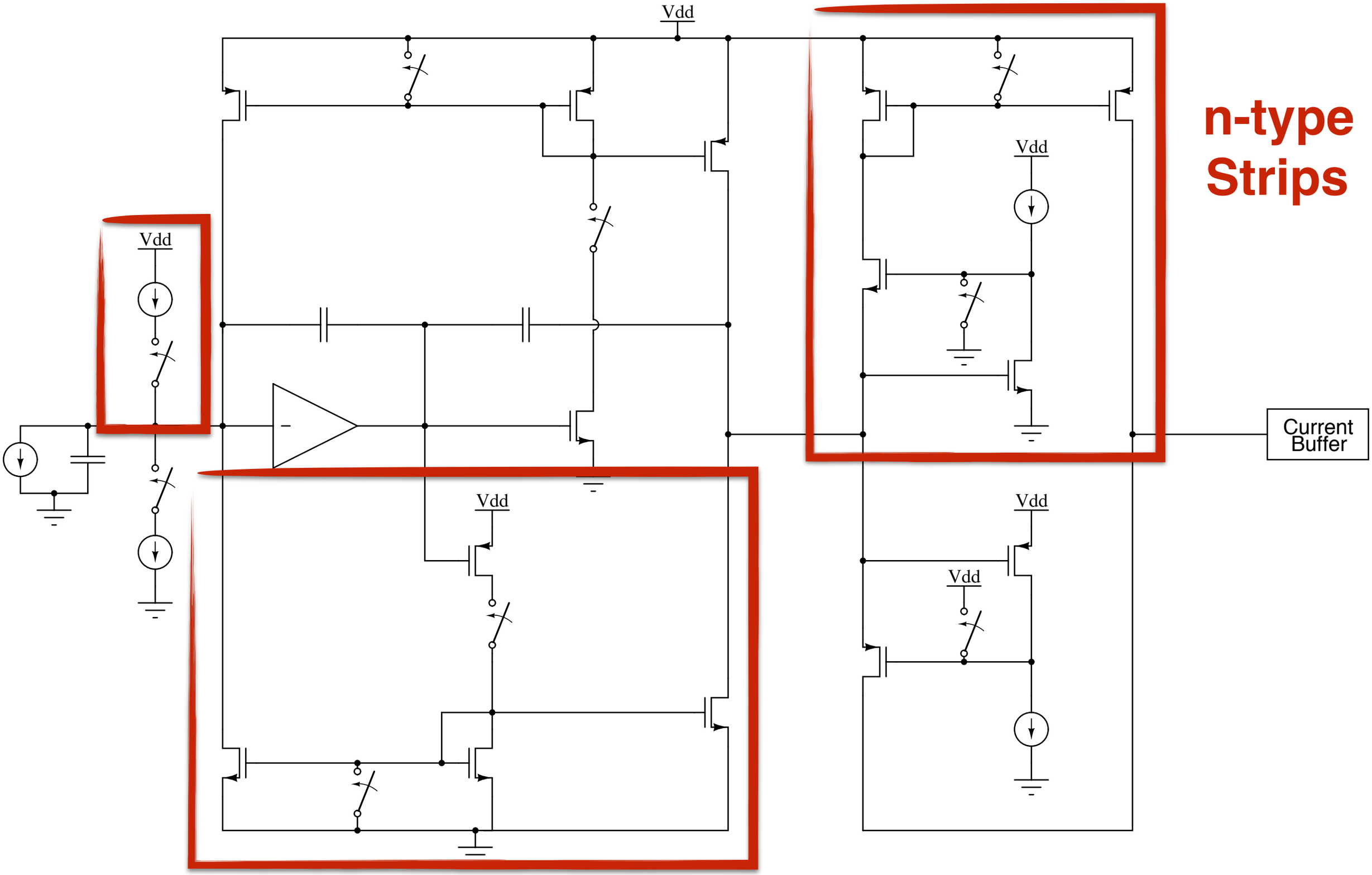


Preamplifier



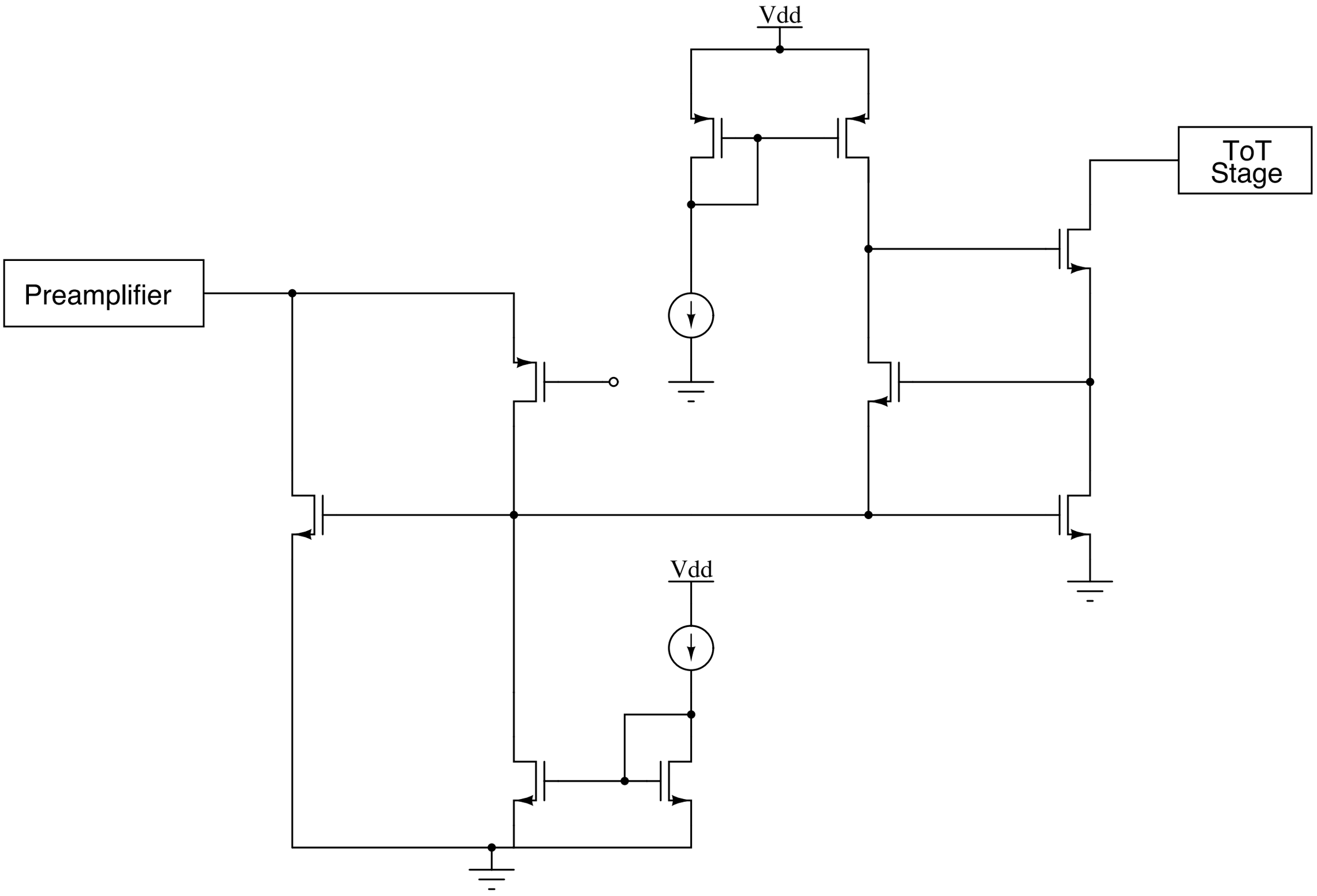
p-type Strips

Preamplifier

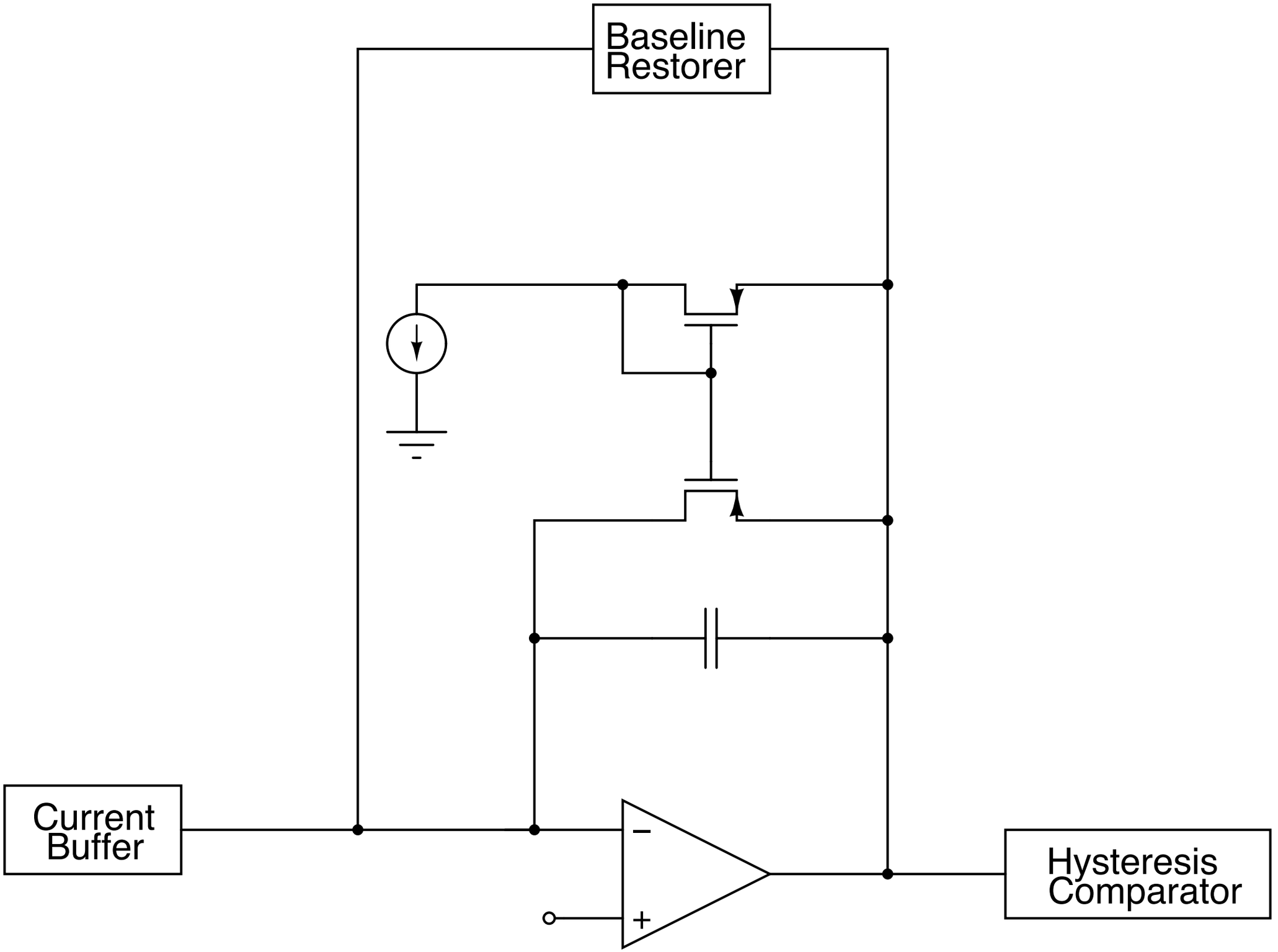


n-type Strips

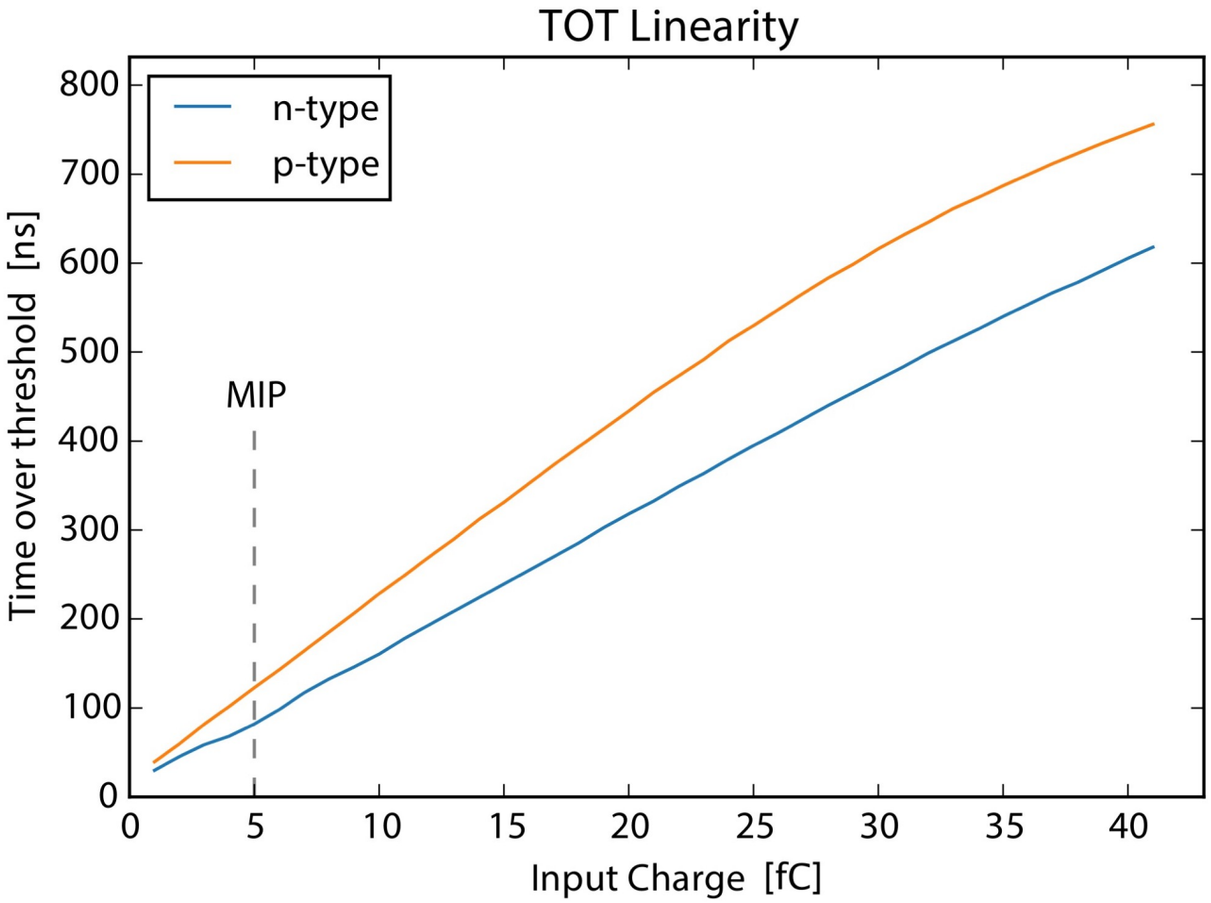
Current Buffer

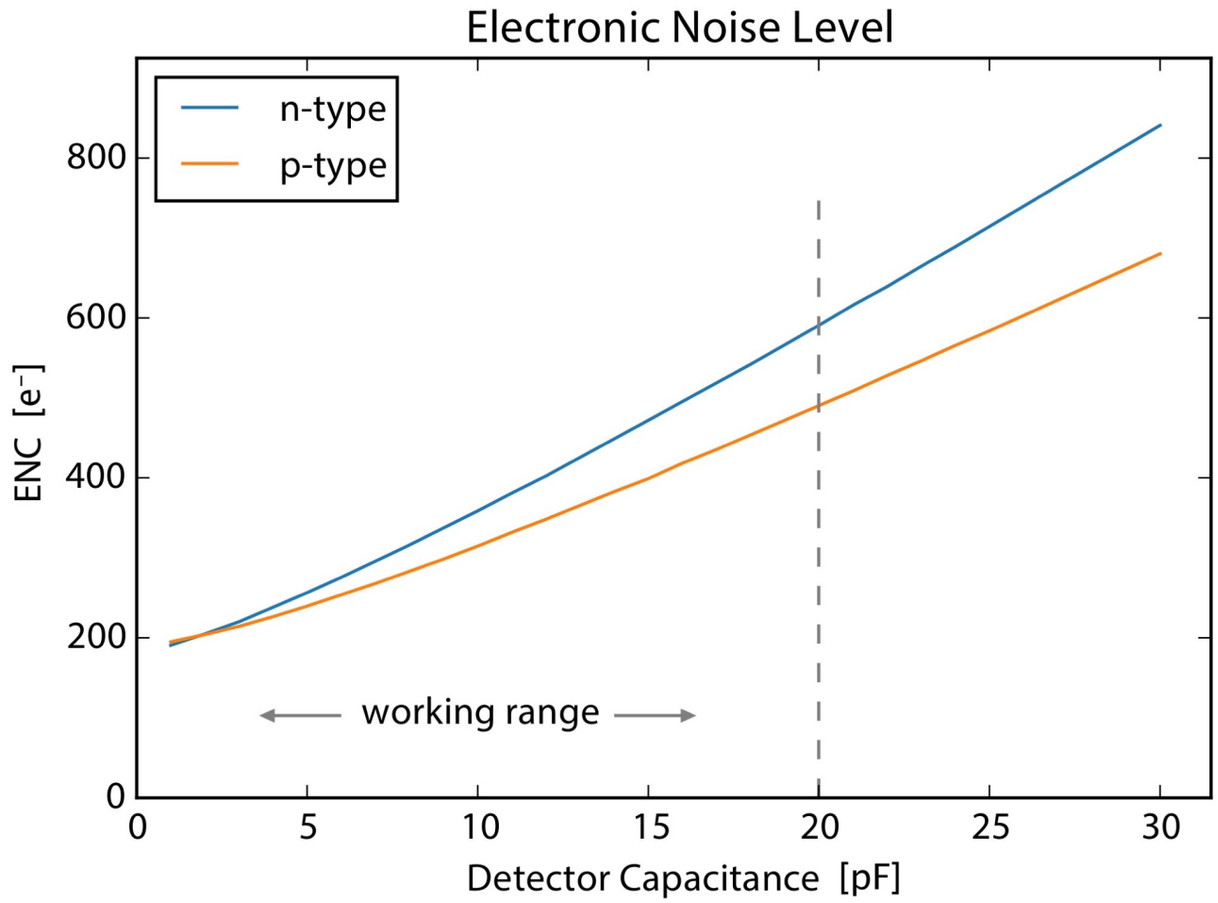


ToT Amplifier

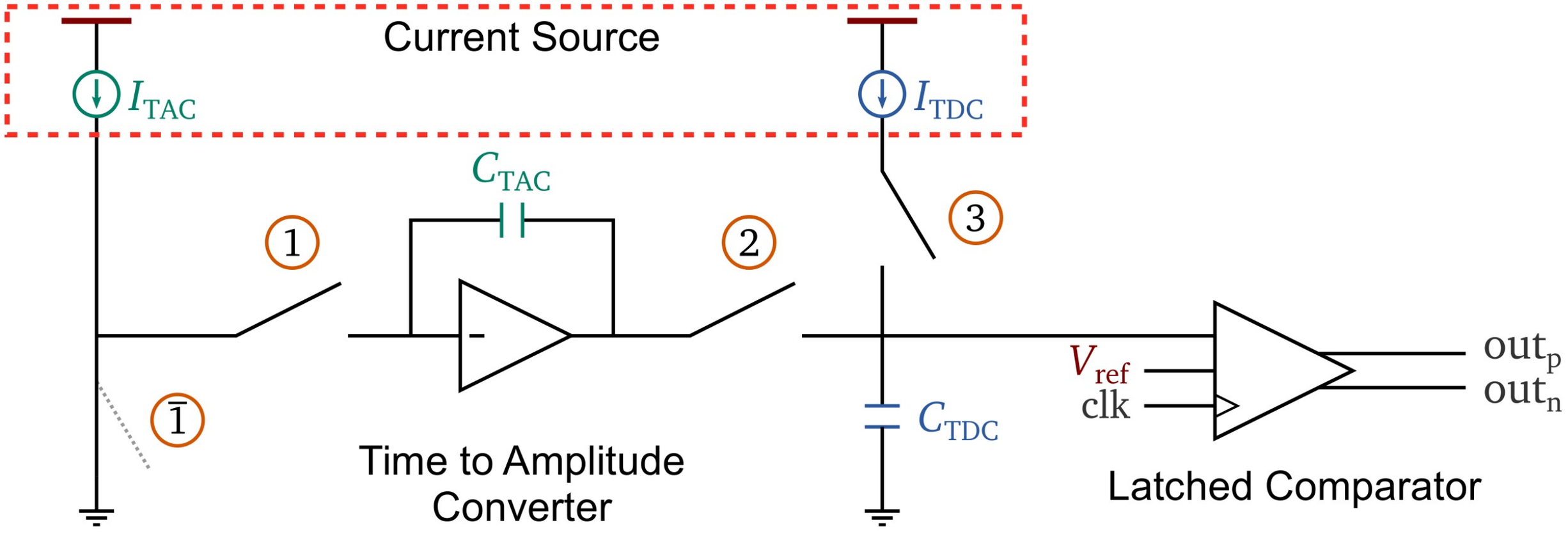


Simulations

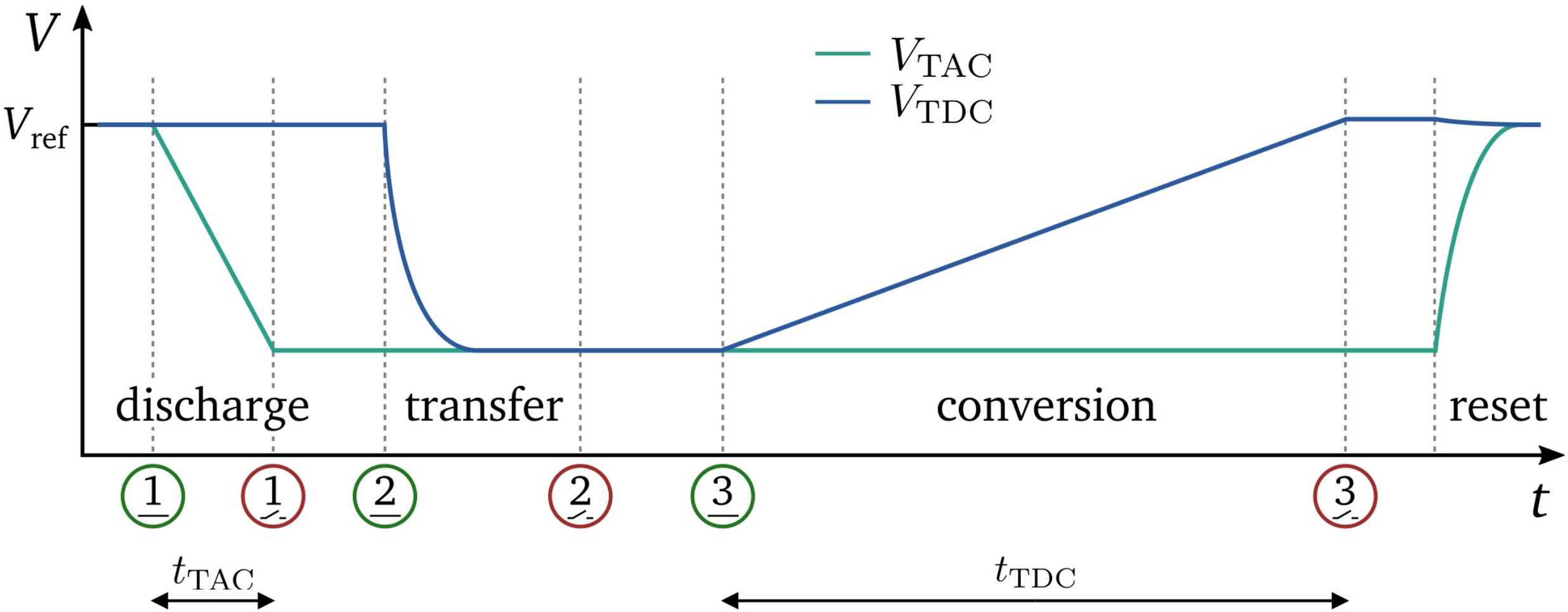




Analog TDC


Current Source
I_{TAC}
I_{TDC}
C_{TAC}
1
2
3
$\bar{1}$
Time to Amplitude Converter
C_{TDC}
V_{ref}
clk
out_p
out_n
Latched Comparator

Time Amplification



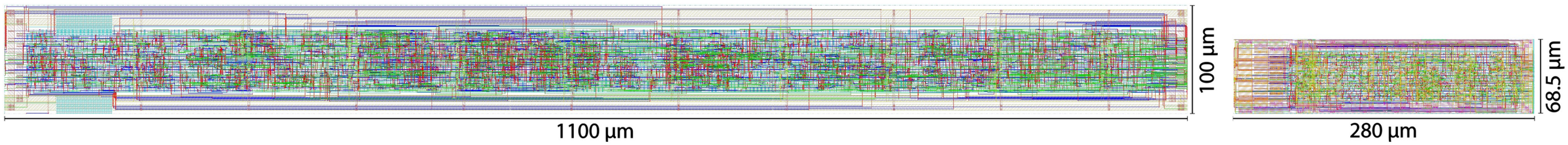
$$C_{\mathrm{TDC}} = 4 \cdot C_{\mathrm{TAC}}$$

$$I_{\mathrm{TDC}} = {}^{1}/_{32} \cdot I_{\mathrm{TAC}}$$

$$V_{\mathrm{TDC}} = V_{\mathrm{TAC}} \Longleftrightarrow \frac{I_{\mathrm{TDC}} \cdot t_{\mathrm{TDC}}}{C_{\mathrm{TDC}}} = \frac{I_{\mathrm{TAC}} \cdot t_{\mathrm{TAC}}}{C_{\mathrm{TAC}}} \Longrightarrow t_{\mathrm{TDC}} = 128 \cdot t_{\mathrm{TAC}}$$

Digital Blocks

- Optimization of the TDC Control
  - Size reduced by ~ 80%
  - Overall power consumption halved
  - Radiation-hard logic implemented



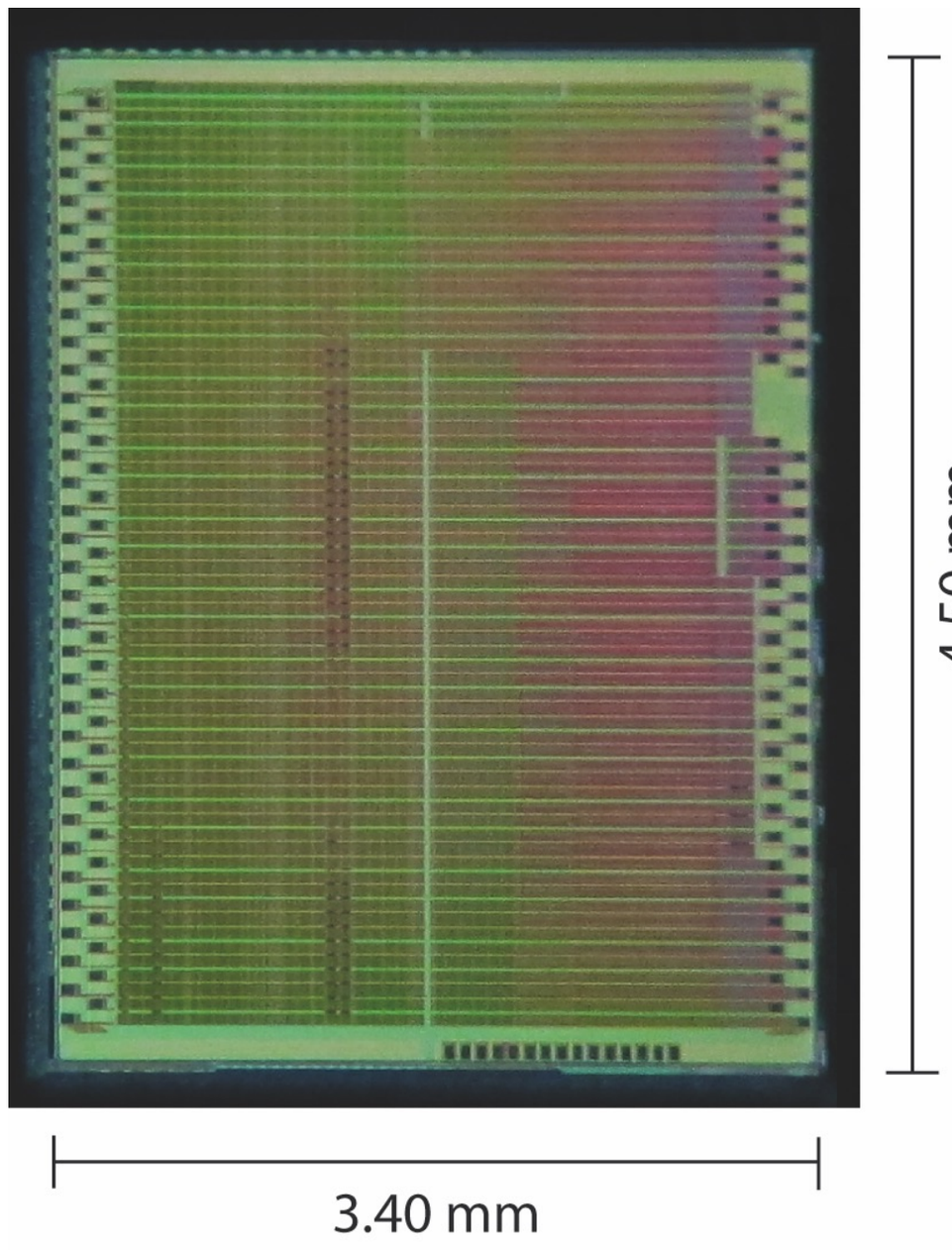
- Single Event Upset (SEU) Protection
  - 1 bit: Triple Modular Redundancy
  - n bits: Hamming encoding

Conclusions

- Chip designed according to the given specifications

- Project submitted in April 2015

- Prototypes delivered in September 2015



Perspectives

- Readout System under development
- PCB design started
- Beam test planned for early 2016

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Thank You

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